Silicon Drift Detectors

A thesis submitted for the degree of
Master of Technology
in the **Faculty of Engineering** by

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Contents

List of Tables

List of Figures

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First, I would like to thank my advisor Professor Sushobhan Avasthi for his guidance during the course of project.

Then, I would like to thank my mother, sister and Nana-Nani for taking care of me in hard times.

Abstract

Silicon drift detectors (SDDs) are used in high-resolution and high-count-rate X-ray spectroscopy. SDDs have application in high-energy physics for particle tracking and in astronomy for telescopes. SDD with high-resolution and low leakage, require optimized device design. This thesis presents a study of circular (cylindrical) SDD, for X-ray spectroscopy using TCAD simulations. Influence of different biasing schemes and device geometry are presented. Device design is optimized on three performance metrics - low leakage current, low anode capacitance and high radial drift field. Capacitance variation due to fringe effects is studied. Limitations on biasing voltages due to punch through are explored. To evaluate uniformity and strength of drift field, concepts of drift channel and mean drift field along the drift channel are introduced which qualify the performance of device. Different surface potential profiles are evaluated considering mean drift field and uniformity as criteria. Finally, large area cylindrical SDD of thickness 1000 µm and radius 5000 µm is presented with leakage current limited to bulk generation current (100 nA), capacitance less than 100 fF and mean drift field of 600 V/cm.

Chapter 1

Introduction

1.1 Basics of X-ray detection

After striking a material, X-ray photon interacts with the nucleus and electrons in the material. The interaction takes place due to one of these three physical processes , namely, **photoelectric effect**, **compton scattering** and **Rayleigh scattering**

For most of the materials used for X-ray detection, photoelectric effect is the dominant process for X-ray energy below 100 keV. Photoelectric absorption in a material increase with atomic number (Z).

In an X-ray detector, the aim is to absorb all the energy of the X-ray photon in the detector material. After complete absorption within the material, energy of the incident X-ray photon is converted into proportional amount of charge (electrical signal) which travels within the detector towards the output electrode. Processing of the signal is done to get information about energy and arrival time of the incident X-ray photon.

1.1.1 Energy to charge conversion efficiency

The number of electron hole pairs (Q) generated per unit energy (E) of incoming radiation is defined by $\epsilon = \frac{E}{Q}$. The factor ϵ tells the granularity (or resolution) of energy measurement of incident X-ray. Lower ϵ means less energy is required to generate charge and so more amount of charge(signal) is generated for same amount of energy. This means increased sensitivity and higher resolution in energy measurement. ϵ is 3.6 eV for Silicon while in Argon it is 26 eV showing Silicon based detectors have better intrinsic resolution than Argon based gas detectors. [2]

1.1.2 Absorption efficiency

As X-ray travels across a material, its energy decreases by a factor called attenuation (or absorption) coefficient per unit length. Absorption coefficient determine how much fraction of X-ray energy can be transferred to the material. Absorption coefficient for Si (for energy above 1 keV) is shown in 1.1. It can be seen that absorption coefficient decreases as energy of incident radiation increases. So, thickness of absorbing material should increase to absorb a significant fraction of higher energy X-rays. A kink in the absorption coefficient is seen at about 1.8 keV. This corresponds to K-shell ionisation energy of Si.

$$\frac{dE}{dx} = -\alpha x$$

$$E_{absorbed} = E_{incident}(1 - e^{-\alpha x})$$

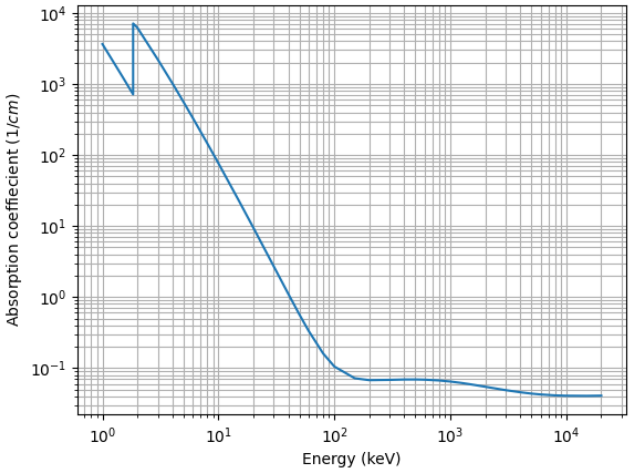


Figure 1.1: Absorption coefficient of Si used for X-ray detection.[1]

For 1000 μm wafer, it can be seen from 1.2 that absorption efficiency is above 90% for energy below 15 keV. So, 1000 μm is suitable for energy detection upto 20 keV.

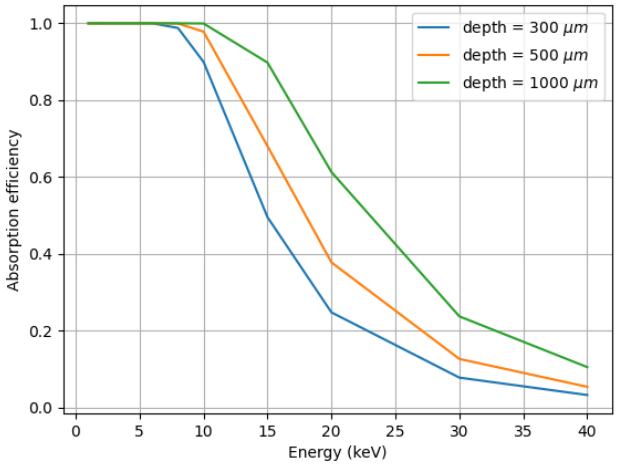


Figure 1.2: Absorption efficiency increasing with wafer thickness

1.1.3 Fano limit

There is an intrinsic energy resolution limit placed by variance in number of generated charge carriers. So, charge conversion efficiency described above is actually average number of charge carriers generated per unit energy. Actually, the number of charge carriers fluctuate and number of charge carriers generated in the semiconductor follow modified-poisson distribution [4] with

$$\sigma = \sqrt{F \times N}$$

where F is the Fano factor and N is number(average) of generated charge carriers

So,

$$N = \epsilon E_0$$

where ϵ is charge conversion efficiency and E_0 is energy of incident radiation

$$\sigma = \sqrt{F \epsilon E_0}$$

$F = 0.115$ for Silicon. It can be seen that σ increases with energy. So, energy resolution is specified by FWHM at some reference energy. Generally, Mn Kα (which is at 5.9 keV) is chosen as reference.

For Silicon, $\sigma \approx 83$ eV at Mn Kα given by Fano limit.

1.2 Working principle of Silicon Drift Detectors

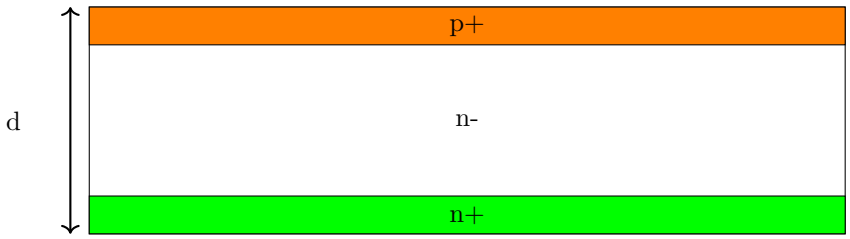


Figure 1.3: Representation of PIN diode (p+-n-n+) (I-region is lightly n-doped layer)

Silicon Drift Detector(SDD) was proposed by Gatti and Rehak [5] in 1984. Since then, SDDs have been improvised in many different ways according to the application. The main advantages of SDDs are high count rate and better energy resolution with respect to other X-ray detectors due to the extremely small anode area and output capacitance.

The working principle of the SDDs can be understood by improvising the design of simplest semiconductor photo-detector - PIN photo-diode which operates under reverse bias. In PIN diodes, complete thickness of Si wafer is available for detection.

Consider PIN diode in figure **??**. It consists of $p+$ region at the top from where light comes in and then generates electron-hole pairs in the $n-$ region where they are separated by electric field and holes are collected at p+ and electrons are collected at n+ contact.

Region near the contact is made highly doped to form good ohmic contact at metal-semiconductor junction which is required for full contribution of collected carriers to electrode current. There is another advantage of high doping at the contact which is low diffusion current. Low diffusion current ensures total leakage current is only limited by generation current (thermal generation at surface and in bulk). Also, thickness of high doped region at entrance window should be small enough so that very small number of carriers are generated there. This is the dead volume of the detector because electron generated experience no electric field and are not collected at n+ contact. This is particularly important for low-energy radiation which gets absorbed close to the surface.[6]

Since the entire thickness is used for photo-detection, n- doped region needs to be fully depleted. So, reverse bias voltage applied should be large enough to dry the carriers in the device.

$$d = \sqrt{\frac{2\epsilon_{Si}(V_{bi} + V_{depletion})}{qN_D}}$$

$$\implies V_{depletion} = q\frac{N_D d^2}{2\epsilon_{Si}} - V_{bi}$$

where N_D is donor density of $n-$ region and d is depletion width (thickness of diode), ϵ_{Si} is dielectric permittivity of Silicon, V_{bi} is the built-in potential due to diffusion at the p+-n junction.

V_{bi} for Si is less than 1.1 V which is much smaller than applied external voltage and hence can be ignored.

This can also be related to resistivity of wafer.

$$\rho = \frac{1}{q\mu_n N_D}$$

where ρ is bulk resistivity of Si, μ_n is the electron mobility and N_D is bulk doping of Si.

From above relation, it is clear that higher resistivity implies lower bulk doping and hence lower depletion voltage.

C-V measurements can be made to find full depletion voltage of the detector. Capacitance of the PIN diode can be given by parallel plate capacitance as depletion region contains two charge layers separated by depletion width.

$$C = \frac{A\epsilon_{Si}}{W_{dep}} = A\sqrt{\frac{q\epsilon_{Si}N_D}{2V_{applied}}}$$

where A is the area of diode

But, after full depletion, depletion width cannot grow and capacitance becomes constant as W_{dep} becomes diode thickness. PIN diodes have lower capacitance compared to ordinary p-n junction due to the large thickness of the i-layer compared to the depletion width of p-n junction. But capacitance of PIN diodes becomes increases with increasing detector area.

To minimise electronic noise (and hence improve energy resolution) and achieve higher count rate, capacitance of detector needs to be minimised. SDDs achieve this with same detection volume as a PIN diode.

SDDs are based on the principle of sideward depletion. This is based on the realisation that ohmic n+ contact on the wafer does not need to extend over full area and can be placed anywhere on the undepleted conducting bulk. This gives us the space to put p+ doped regions on both sides of the wafer so that p-n junctions can be made on both sides. At small voltages applied to n+ electrode, depletion region starts to form on both sides of wafer due to reverse biased p+-n junction (n is shorted to n+ by conducting bulk). At sufficiently high voltage, two space charge regions touch each other and finally whole wafer gets depleted. When the wafer gets fully depleted, a electron potential valley forms in center of the wafer extending from n+ contact.

After radiation enters the detector,generated holes inside the depletion region will be drifted to the p+ contacts while electrons move to the potential valley and then they move slowly towards the anode. If an electric field is applied parallel to the surface, electron drift velocity is higher and then electron collection time is smaller. This can be achieved by diving top p+ layer into strips and applying different voltage to the p+ strips with the most positive nearest to n+ contact.

So, even with small n+ electrode, charge collection from complete wafer is possible. With small n+ electrode, very low capacitance in sub pF range can achieved for large area detectors.

The top view and cross-sectional view of cylindrical SDD considered in this project are shown in 1.5 and 1.6.

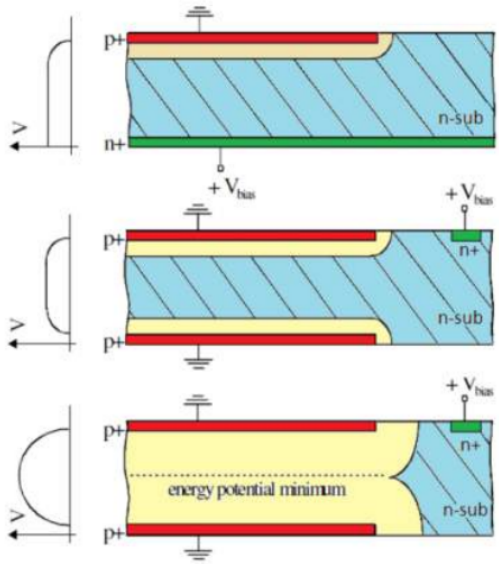


Figure 1.4: Structure demonstrating sideward depletion.[2]

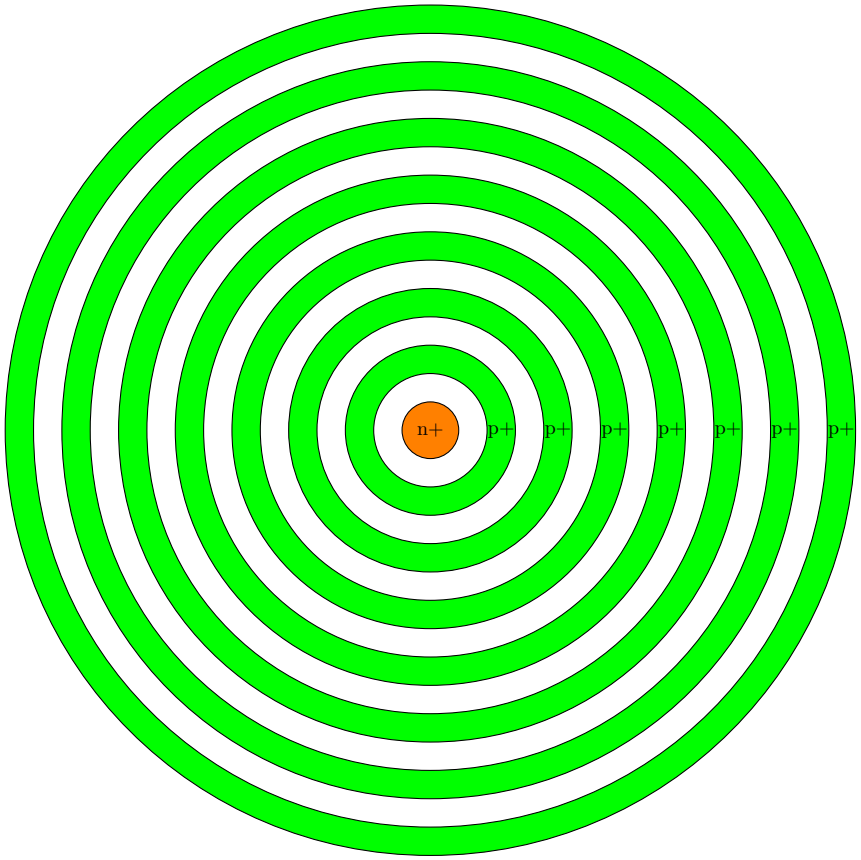


Figure 1.5: Top view of cylindrical SDD

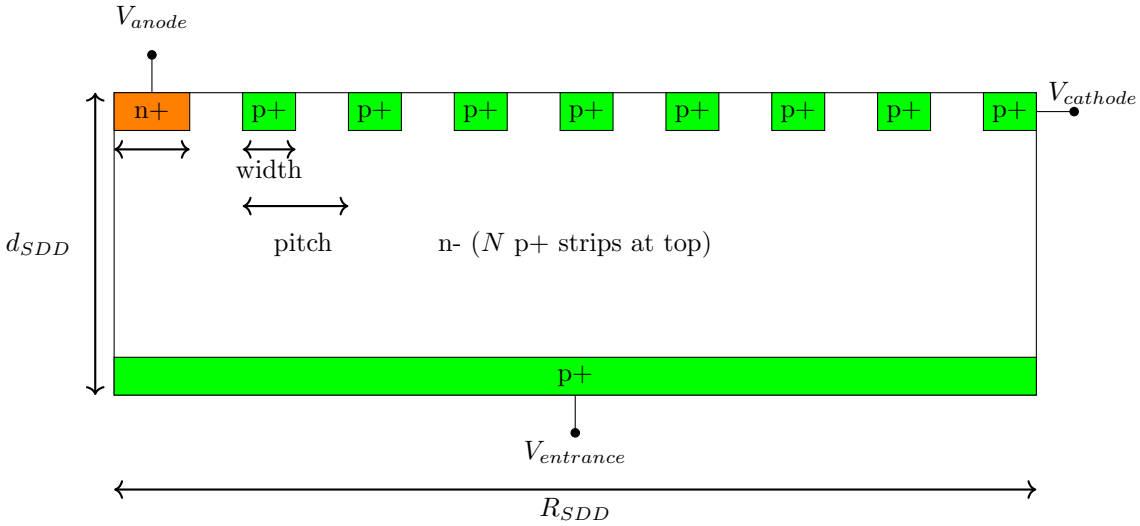


Figure 1.6: Radial cross-section of cylindrical SDD

Chapter 2

Detector parameters

In this chapter, various detector parameters like leakage current, breakdown voltage, drift time and noise are discussed.

2.1 Breakdown voltage

Breakdown voltage is the maximum applied reverse bias voltage which can be applied to a detector before leakage current starts to increase rapidly with applied voltage. Breakdown voltage sets the upper limit of voltage bias as leakage current noise is higher than optical generation above breakdown voltage.

2.1.1 Avalanche breakdown

Avalanche multiplication (or impact ionisation) is the most important mechanism of junction breakdown for PIN diodes. It occurs due to charge carriers accelerated under high electric field near the junction colliding with other charge carriers leading to carrier multiplication. Requirement for avalanche breakdown is high electric field for sufficiently long distance.

Avalanche breakdown voltage for one-sided abrupt planar Si p-n junction diode [7] can be estimated by :

$$V_{BD} = 60 \left(\frac{N}{10^{16}} \right)^{-\frac{3}{4}} V$$

where N is the doping density of lightly doped side

So, V_{BD} increases with doping density of substrate.

For PIN diode, similar estimate can be made if V_{BD} is less than full depletion voltage because the above estimate is made assuming that depletion width at V_{BD} is less than diode thickness. This is true for sufficiently high doped substrate but for PIN diode with low bulk doping, depletion voltage is lower than V_{BD}. So, breakdown voltage is lower than V_{BD}. So, decreased breakdown voltage $V_{BD}^{'}$ is given by

$$V_{BD}^{'} = V_{BD} \frac{W}{W_D} \left(2 - \frac{W}{W_D} \right)$$

where W is the thickness of diode,W_D is given by

$$W_D = \sqrt{\frac{2\epsilon V_{BD}}{qN_D}}$$

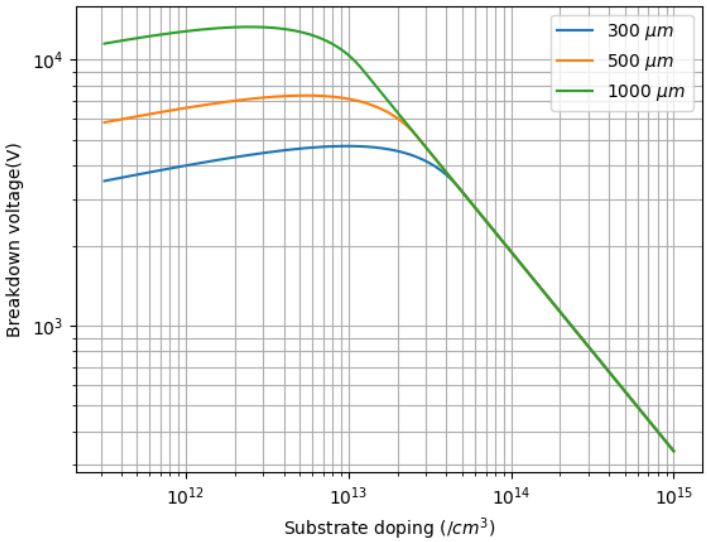


Figure 2.1: Avalanche breakdown voltage increases with detector thickness (PIN diode)

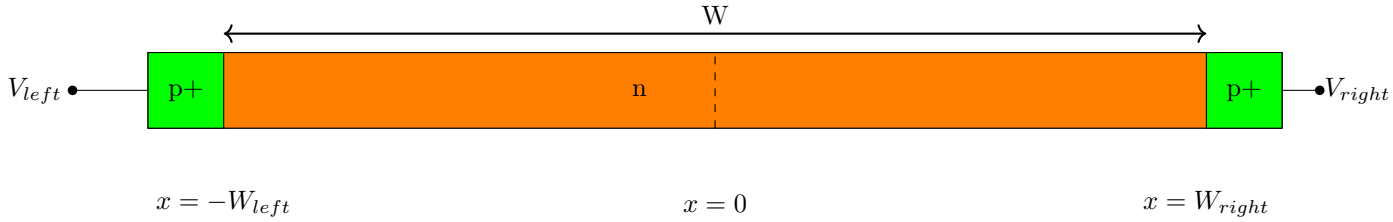


Figure 2.2: One dimensional section of a p+-n-p structure

Avalanche breakdown voltage in 2.1 are for junctions with no curvature (infinite radius of curvature). With curvature introduced, breakdown voltage goes down with increasing curvature because of higher electric field at points of sharp edges. The decrease depends on $\frac{r}{W_D}$ where r is radius of curvature at junction point and can significantly lower breakdown voltage.

2.1.2 Punch-through breakdown

Punch-through breakdown occurs in p+-n-p and n+-p-n structures when depletion region covers whole low doped region and barrier for carrier injection from a highly doped side becomes sufficiently small. Then, carriers are injected over the barrier with the probabilty $e^{\frac{-V_{barrier}}{k_B T}}$ and then swept away by electric field in the bulk.

To understand punch through condition, consider a p+-n-p+ section in 2.2. The section is a part of 2-D structure where n is connected to n+. n+ contact is biased such that whole of the n-region between both p+ regions is depleted.

Considering variation of electric field perpendicular to the x-axis negligible, poisson equation can be written as:

$$\frac{d^2V}{dx^2} = \frac{qN_D}{\epsilon}$$

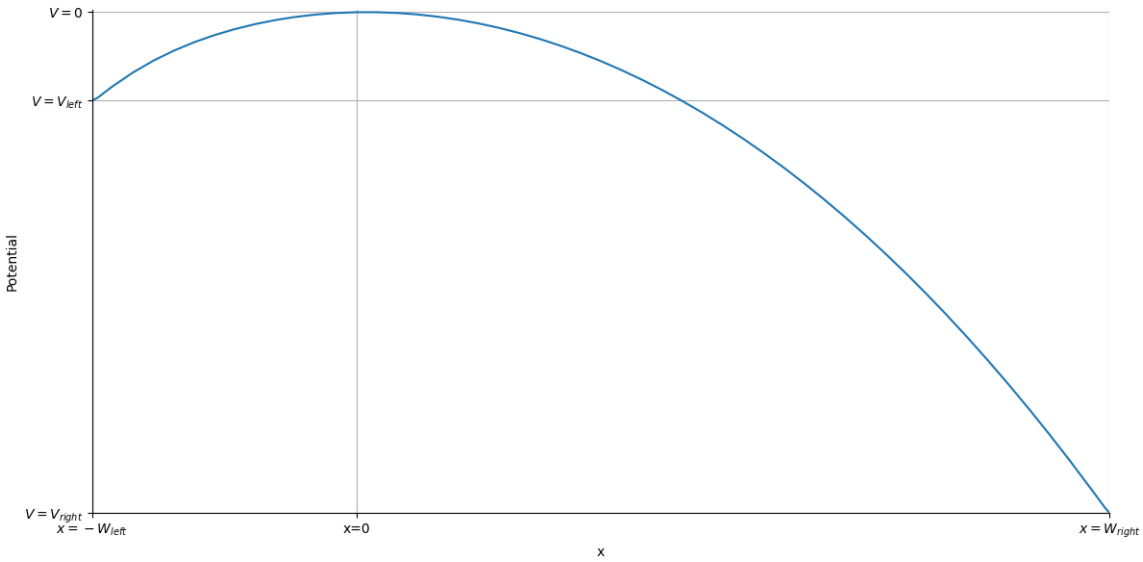


Figure 2.3: Potential profile of p+-n-p structure showing potential barrier for holes (Left end is $x = -W_{left}$ and right end is $x = W_{right}$)

For depletion to be stable, both p-n junctions need to be reverse biased. So, electric field at both junctions are opposite to each other. So, electric field is zero at a point in between them which is the potential maxima. At that point, $x = 0$ and $V = 0$ are set as reference.

Since both p-n junctions are reverse biased, electric field in depletion region of one is opposite to other. So, there lies a point where electric field is 0. $|V_{left}|$ and $|V_{right}|$ represent the barrier for holes on left and right p-n junctions respectively.Let $\Delta V = V_{left} - V_{right}$.

Under full depletion,

$$V_{left} = -\frac{qN_D W_{left}^2}{2\epsilon}$$

$$V_{right} = -\frac{qN_D W_{right}^2}{2\epsilon}$$

$$\implies V_{left} + V_{right} = -\frac{qN_D(W_{left}^2 + (W - W_{left})^2)}{2\epsilon}$$

Sum of barriers is minimum when they are equal and maximum when one of them is 0. So,

$$\implies V_{dep} \geq |V_{left}| + |V_{right}| \geq \frac{V_{dep}}{2} \tag{2.1}$$

$$\Delta V = V_{left} - V_{right} = \frac{qN_D}{2\epsilon}(W_{right}^2 - W_{left}^2) = \frac{qN_D}{2\epsilon}(W_{right} - W_{left})(W_{right} + W_{left})$$

$$\implies \Delta V = \frac{qN_D}{2\epsilon}(W_{right} - W_{left})W$$

$$\implies W_{right} - W_{left} = \frac{2\epsilon\Delta V}{qN_D W}$$

$$W_{right} + W_{left} = W$$

where $V_{dep} = \frac{qN_D W^2}{2\epsilon}$

$$\implies W_{left} = \frac{W}{2} - \frac{\epsilon\Delta V}{qN_D W}; W_{right} = \frac{W}{2} + \frac{\epsilon\Delta V}{qN_D W} \tag{2.2}$$

So, (from (2.2)),as ΔV increases, barrier moves towards left p+ region and also decreases in height near left p+. Under full depletion, ΔV can't be greater than depletion voltage. If ΔV is increased beyond V_{dep} , holes are injected from p+ to the bulk and breakdown occurs.

Punch-through breakdown, for silicon drift detectors, often occurs before avalanche breakdown and sets the limiting voltage to device operation. In SDD, biasing is done such that punch-through does not happen between p+ strip on n-side and p+ layer on p-side.

In this one-dimensional description, it is assumed that electric field variation (actually net electric flux crossing perpendicular to the axis of the junction) is negligible in other dimension. This may be not always true. Variation of electric field perpendicular to the axis may lead to increase or decrease of breakdown voltage between p+ electrodes.

Punch-through breakdown is discussed by simulation of SDD in chapter 3.

2.2 Dark Current (Leakage Current)

One of the important aspects of semiconductor detector design is low dark current (leakage current). Dark current is the current flowing through the detector in absence of any light shining on it. This is a source of noise and adds to the signal current. So, reducing it is necessary to get correct quantitative estimation of energy dose of the radiation.

There are two major sources contributing to the dark current - **Diffusion Current** and **Generation Current**

2.2.1 Diffusion Current

Diffusion current flows due to carrier density gradient. In a reverse biased pn-junction, diffusion current is produced by diffusion of minority carriers from quasi-neutral regions of the detector towards the depletion region which are then swept towards the electrode by the electric field to the other side of the junction. Diffusion current depends on diffusion coefficient (mobility), length of quasi-neutral region, background doping and temperature.

$$J_{diffusion} = q\left(\frac{{n_i}^2}{N_D}\frac{D_p}{L_p} + \frac{{n_i}^2}{N_A}\frac{D_n}{L_n}\right)(1 - e^{\frac{qV}{kT}}) \tag{2.1}$$

where V,$J_{diffusion}$, D_p and D_n are applied reverse bias,diffusion current density,electron and hole diffusion coefficients respectively.

D can be estimated by Einstein relation.

$$D = \mu\frac{kT}{q}$$

For long diodes (length of diode is much larger than diffusion length), L_p and L_n are given by diffusion length given by

$$L_p = \sqrt{D_p \tau_p}$$
$$L_n = \sqrt{D_n \tau_n}$$

where τ_p and τ_n are hole and electron SRH recombination lifetimes respectively.

For high quality FZ wafers, carrier lifetimes are above 1 ms which leads to diffusion length of about $1 - 2$ mm.

However, semiconductor detectors operate in full depletion mode. Since the detectors are completely depleted and the high doped layers are implanted at very shallow depths to keep dead volume very low, p+-n junctions act as short diodes where quasi-neutral region length is equal to implantation depth. L_p and L_n are simply given by quasi-neutral region of undepleted highly doped regions near ohmic contact. So, this means diffusion current cannot be reduced below a certain threshold just by increasing lifetime.

Since depletion voltage is very high compared to thermal voltage, exponential term can be neglected and diffusion current density at full depletion is given by the constant term in (2.1)

$$J_{diffusion} = q \left(\frac{{n_i}^2}{N_D} \frac{D_p}{L_p} + \frac{{n_i}^2}{N_A} \frac{D_n}{L_n} \right)$$

Diffusion current can be limited by cooling the detector because of exponential dependence of the current on temperature.

Consider a PIN diode with L_p and L_n both equal to 1 μm and $N_D = N_A = 10^{18}/cm^3$ at ohmic contacts. Bulk doping of the substrate is $10^{12}/cm^3$. D_p is 12 cm^2/s and D_n is 36 cm cm^2/s.

Then , diffusion current at full depletion is given by (**??**).

$$J_{diffusion} \approx \ 16pA/cm^2$$

2.2.2 Bulk generation current

Bulk generation current is due to thermal generation of carriers within the detector. In a reverse biased pn-junction, in depletion region, carrier densities are very low and below the equilibrium carrier densities. This causes thermal generation of electron-hole pairs in the depletion region. Thermal generation rate can be estimated by SRH generation rate (assuming single trap state at intrisic fermi-level energy) given by:

$$G = \frac{n_i^2 - pn}{\tau_n(p + n_i) + \tau_p(n + n_i)} \tag{1.4}$$

where G is bulk generation rate, τ_n and τ_p are SRH carrier lifetimes.

For fully depleted regions, $n, p << n_i$. The generation rate can be approximated as :

$$G = \frac{n_i}{\tau_n + \tau_p} = \frac{n_i}{\tau_g} \tag{1.5}$$

where $\tau_g = \tau_n + \tau_p$ is generation lifetime

Multiplying generation rate by depletion width and charge leads to generation current density

$$J_{generation} \approx qGW_{dep} = qn_i \frac{W_{dep}}{\tau_g}$$

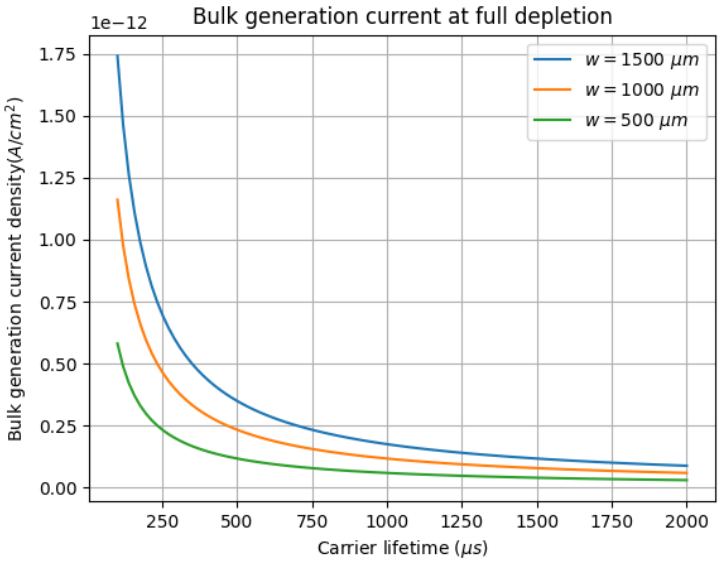


Figure 2.4: Bulk generation current increases with detector thickness at full depletion

where τ_g is generation lifetime and W_{dep} is depletion width.

For cylindrical detectors, bulk generation current under full depletion can be estimated by multiplying detector volume with bulk generation rate. For fully depleted detectors,

$$G = \frac{n_i}{\tau_g} \approx \frac{n_i}{\tau_p + \tau_n} = \frac{n_i}{2\tau} \; for \; \tau_p = \tau_n = \tau$$
$$I_{gen} = G \times Volume \; = G \times \pi r^2 d = q\frac{n_i}{2\tau}\pi r^2 d$$

where d is detector thickness and r is radius of detector

Consider $\tau_p = \tau_n = 1 \; ms$ and $W_{dep} = 500\mu m$. For depleted semiconductor, generation lifetime $\tau_g \approx \tau_p + \tau_n$. Then,

$$\tau_g = 2ms$$
$$I_{generation} \approx 58 \; nA/cm^2.$$

This shows that (compare with diffusion current),for semiconductor detectors, bulk generation current dominates the current even for carrier lifetimes as high as 1 ms as diffusion current is very small due to very high doped regions limiting diffusion current.

For partially depleted semiconductors,

$$W_{dep} = \sqrt{\frac{2\epsilon V}{qN_D}} \tag{2.3}$$

$\sqrt{V}$ dependence of W_{dep} serves as the verification of the reverse biased current being generation dominated. Also, after full depletion, current does not increase because dark generation rate can't increase.

2.3 Collection efficiency

Collection efficiency of a detector is the fraction of generated charge collected at the detector electrodes. Collected charge can be estimated by integrating signal current over signal period removing the contribution from dark leakage current.

$$Q_{collection} = \int_0^{t_0} (I - I_{dark}) dt$$

where t_0 is signal width

Then collection efficiency η is given by:

$$\eta = \frac{Q_{collection}}{Q_{generation}}$$

2.4 Transient behaviour

Due to the energy deposited by incident radiation, electron-hole pairs are created within the detector which induce charge on the detector electrodes. From the time charge carriers are created, signal in form of charge induced starts to appear on output electrodes. The signal ends when the all the generated charges are collected at the electrodes. While a charge moves from generation point to the electrode, trajectory of charge carriers along with the geometric arrangement of electrodes decide the output signal generated on the output electrode.

From linear superposition of electric field, electric field at the electrodes can be written as sum of two electric fields - electric field only due to bias potentials and space charge and electric field only due to generated charge. Then, charge at the electrodes can be separately attributed to two components of electric field. Then, total charge Q and induced charge Q_i can be written as

$$Q = \oiint \epsilon \vec{E}.d\vec{S}$$
$$Q_i = \oiint \epsilon \vec{E}_{gen}.d\vec{S}$$

where $\vec{E}$ and $\vec{E}_{gen}$ are net electric field and electric field due to generated charge respectively.

This shows induced charge is independent of bias potentials and space charge.

2.4.1 Shockley-Ramo Theorem

The Shockley–Ramo theorem [8] [9] [10] can be stated as: The charge Q and current i on an electrode induced by a moving point charge q are given by:

$$Q = -q\ \phi_0(\mathbf{x})$$
$$i = -q\ \vec{v}.\vec{E_0}(\mathbf{x})$$

where $\vec{v}$ is the instantaneous velocity of charge q, and $\phi_0(\mathbf{x})$, $\vec{E_0}$ are the electric potential and field that would exist at q's instantaneous position $\mathbf{x}$ under the following circumstances: the selected electrode at unit potential, all other electrodes at zero potential and all charges removed.$\phi_0(\mathbf{x})$ and $\vec{E_0}$ are called the weighting potential and the weighting field, respectively.

While the trajectory of the charge q is determined by the actual operating electric field, the induced charge Q can be calculated much easily with the help of the weighting potential. The weighing potential only depends on geometry of the system and is independent of actual bias potentials.

Shockley-Ramo Theorem can be understood as a result of applying conservation of energy to system of generated charge, detector and power supply with the following argument. So, after generation, as charge moves within the device, it gains velocity and hence kinetic energy. The kinetic energy gain comes from electric field within the detector ($v = \mu E$ for semiconductors). So, to restore that electric field,extra energy (other than power only due to is pumped into the detector by power supplies. The energy supplied is seen in form induced charge on electrodes due to the capacitance($E = \frac{Q^2}{2C}$) (or increased current meaning higher power consumption). After generated charge is collected, the induced charge also vanishes.

One can also see agreement between Shockley-Ramo Theorem and conservation of charge with the following arguments. Weighing potential can be calculated for each electrode by applying unit potential to that electrode and grounding others. By using superposition principle, sum of all weighing potentials would be potential for all electrodes at unit potential. Since potential has only relative value, this solution is equivalent to all electrodes grounded leading to weighing potential zero everywhere and hence net induced charge being zero.

2.4.2 Drift time

Drift time of the detector is the time required by generated carriers within the detector to reach the contact electrodes. The signal generated at the electrode reaches its maximum value at drift time (from start of signal) and decreases after it as carriers are removed from detector. The drift time can be used to estimate the radial distance to point of generation within the detector.

For electrons, it can be estimated by

$$t = \int_{r_0}^{r} \frac{dr}{v_{drift,r}} = \int_{r_0}^{r} \frac{dr}{\mu_n \; E_{drift,r}} = \frac{r - r_0}{\mu_n \; E_{drift,mean}} \tag{1.4}$$

where

$$E_{drift,mean} = \frac{d}{\int_{r_0}^{r} \frac{dr}{E_{drift,r}}},$$

$r - r_0$ is distance between carrier generation and contact electrode and $v_{drift,r}$ is carrier radial drift velocity dependent on mobility μ_n and radial drift electric field $E_{drift,r}$.

Mathematically,$E_{drift,mean}$ is harmonic mean of E_{drift}.

$$\Delta V = \int E dr.$$

For a given sum, harmonic mean is minimum when all elements are equal. So, a given potential difference at two ends, optimum field is uniform.

Physically,$E_{drift,mean}$ tells us how fast the carriers drift towards the contact. Regions with lower $E_{drift,r}$ determine the value of $E_{drift,mean}$. So, for given biasing voltage on electrodes, uniform $E_{drift,r}$ results in higher $E_{drift,mean}$. So, while designing the detector, uniformity of $E_{drift,r}$ becomes important.

So,$E_{drift,mean}$ can be used to compare timing capabilities of detectors with same dimensions.

2.4.3 Signal spread (in time)

To consider the spread of carriers, consider a one-dimensional semiconductor given in 2.5.

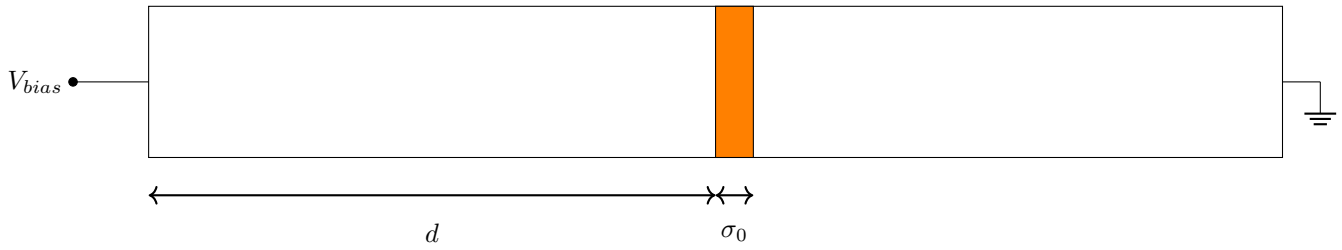


Figure 2.5: Generated charge packet with width σ_0 at distance d

Due to applied electric field, the carriers move(drift) towards their respective electrodes. While they drift,they also diffuse within the detector due to sudden increase of charge setting up carrier density gradients resulting in spread of generated charge cloud. Charge packet width σ at time t after generation can be given by :

$$\sigma^2 = \sigma_0^2 + Dt = \sigma_0^2 + \mu\frac{kT}{q}t$$

where diffusion coefficient is given by

$$D = \mu\frac{kT}{q}$$

Broadened charge packet profile forms a gaussian distribution in space with standard deviation σ. The gaussian distribution is due to finite charge packet diffusion.

Due to charge packet broadening, charge carriers reach the electrode at different times resulting in broadening of signal peak. Then, peak width in time Δt depends on charge packet width and carrier drift velocity

$$\Delta t = \frac{\sigma}{v_{drift}} = \frac{\sqrt{\sigma_0^2 + \mu\frac{kT}{q}t}}{v_{drift}} \tag{2.4}$$

So, from (2.4), if initial packet width is small, Δt is proportional to $\sqrt{t}$.

Note, in addition to signal spread due to diffusion, there will be signal spread due to the induced charge varying as charge carrier moves from point of generation towards the electrode. So, pulse shape predicted by Schokley-Ramo theorem along a defined trajectory (with known electric field) gets broadened (smoothened) by diffusion. Usually, for SDDs, as it will be shown in next chapter, diffusion spread is much larger compared to weighing potential spread.

2.5 Noise in detectors

For a current i flowing through a sample of length d between two electrodes due to n carriers moving with velocity v, weighing field (E_0) and consequently i (by Shockley-Ramo theorem) can be written as:

$$E_0 = \frac{1}{d}$$
$$i = qnvE_0 = \frac{qnv}{l}$$

So, the fluctuation in current can be due to fluctuation in number of carriers flowing and fluctuation in velocity of flowing carriers. Considering the two sources as independent of each other, noise in current due to both sources can be added in quadrature.

$$\langle di \rangle^2 = \frac{qv}{l}\langle dn \rangle^2 + \frac{qn}{l}\langle dv \rangle^2$$

2.5.1 Thermal Noise

Thermal noise is the noise due to velocity fluctuations caused by random thermal motion of carriers due to thermal energy. This fluctuation is in addition to drift velocity due to electric field (generating a constant current). Spectral noise power density for thermal noise is given by :

$$\frac{dP_n}{df} = 4k_B T$$

where k_B is Boltzmann constant and T is the temperature of carriers

Noise power is equivalent to a current source (I_{noise}) in parallel or a voltage source (V_{noise}) in series with spectral densities given by:

$$\frac{dI^2_{noise}}{df} = \frac{4k_B T}{R}$$
$$\frac{dV^2_{noise}}{df} = 4k_B T R$$

In detectors, thermal noise is generated in the biasing resistors connected to the detector.

2.5.2 Shot noise

Shot noise is due to fluctuations in number of flowing carriers within the sample. Shot noise occurs for all quantities which show discrete nature (particle nature). Shot noise exists whenever movement of charge carriers can be modelled as poisson process (movement of a charge carriers is independent of each other). This occurs in semiconductors when carriers are injected from one side of the junction to the other side across a barrier with finite probability. Here, each carrier has same probability of crossing the barrier. Based on poisson statistics, the number fluctuation (Δn) is given by $\sqrt{n}$. Then, the spectral current density is given by:

$$I^2_{shot} = 2qi$$

In detectors, fluctuations in dark leakage current (as thermal generation is a statistical process) leads to shot noise.

2.5.3 Signal to noise ratio (SNR)

This discussion is due to [3].

Consider the detector in 2.6. When generated charge carriers move towards the electrodes, they induce current on the sensor electrodes forming the capacitor C_d. The induced current is integrated on the detector capacitance and input capacitance of amplifier. The signal charge gets distributed between amplifier input capacitance and sensor capacitance. Then, the voltage V_i at the amplifier input is given by:

$$V_i = \frac{Q_s}{C_d + C_i}$$

where Q_s is the signal(induced) charge

So, the input signal is inversely proportional to total sum of sensor capacitance and amplifier input capacitance for given input charge. So, SNR decreases with increasing capacitance. So, low capacitance is desirable for detectors.

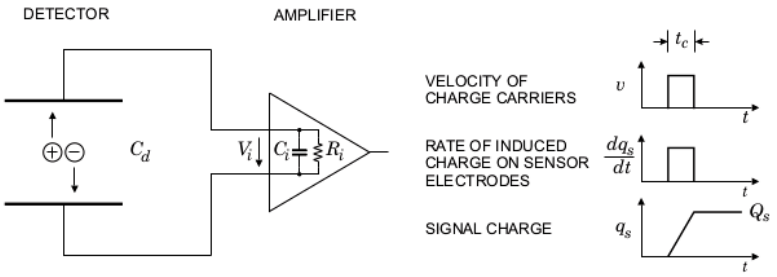


Figure 2.6: Charge collection and signal integration.Diagram from [3]

Chapter 3

Design and Simulations

This chapter discusses design techniques for SDDs and evaluates the different designs (different surface potentials) performing simulations to extract performance parameters.

First, simulation procedure and models are described. Then, capacitance variation with anode radius is discussed. After that, defining the structure and surface potential, comparison is made between different surface potentials on the basis of drift field.

3.1 Simulation methodology

Simulating a semiconductor structure means solving for electrostatic potential and carrier densities in semiconductor using poisson's equation along with electron continuity equation and hole continuity equation under applied bias.

$$\nabla^2\psi = -\frac{q(N_D - N_A + p - n)}{\epsilon}$$
$$R - G = \frac{\vec{\nabla}.\vec{J_n}}{q} - \frac{\partial n}{\partial t} = -\frac{\vec{\nabla}.\vec{J_p}}{q} - \frac{\partial p}{\partial t}$$

where ψ,n,p,J_p,J_n and R are electrostatic potential, electron density, hole density, hole current density, electron current density and recombination rate respectively

Additionally, under drift-diffusion formalism, electron and hole current density are given by

$$\vec{J_n} = n\mu_n\nabla\phi_n$$
$$\vec{J_p} = p\mu_p\nabla\phi_p$$

where ϕ_n and ϕ_p are electron and hole quas-fermi levels respectively defined as

$$\phi_n = k_BT\ ln\frac{n}{n_i} + E_i$$
$$\phi_p = -k_BT\ ln\frac{p}{n_i} + E_i$$

where E_i is intrinsic fermi-level

SRH recombination model is used with constant lifetimes assuming single mid-gap trap state

$$R = \frac{pn - n_i^2}{\tau_n(p + n_i) + \tau_p(n + n_i)}$$

where τ_p and τ_n are hole and electron carrier lifetimes respectively

So, for all simulations, the above equations are solved. Boltzmann statistics is used to approximate carrier statistics. For avalanche breakdown simulation, additional model by Selberr is used with the default parameters defined in SILVACO ATLAS Manual [11].

Initially, a non-uniform smooth mesh is generated dividing the structure into small triangular elements. Mesh is dense generated near the junctions and coarse in the bulk. Mesh spacing is finer than the debye length (L_D) in the critical regions of the devices to properly resolve electric field and carrier density variations. The solver uses finite element method for discretisation. Newton's method is used for solving system of poisson equation and continuity equations.

$$L_D = \sqrt{\frac{\epsilon_{Si} k_B T}{q^2 N_D}} \approx 4\mu m \ for \ N_D = 10^{12} cm^{-3}$$

Since the structure is cylindrical, $r = 0$ is the axis of symmetry and has reflecting boundary conditions. Along with that, all the non-contact boundaries of the simulation domain have reflecting boundary conditions. This means the domain is self contained and there is no electric current flux at non-contact boundaries. Also, there is no electric field perpendicular to the surface at the non-contact boundaries (no charge at the non-contact boundaries). All the contacts are defined ohmic in nature.

Since carrier and current densities are low under reverse bias, all simulations have been performed with 80-bit precision using SILVACO ATLAS solver to avoid noisy solution.

3.2 Capacitance variation with anode radius

For designing low capacitance SDD, anode capacitance simulation of a simplified structure shown in **??** is done.

For parallel plate capacitors with large area A compared to d^2 where d is the distance between the plates is given by

$$C = \epsilon \frac{A}{d}$$

For cylindrical plates with radius r, $A = \pi r^2$.

$$\implies C = \epsilon \frac{\pi r^2}{d} \tag{3.1}$$

where r is radius of capacitor plate

From the above relation, one expects that C is proportional to r^2 for large r compared to distance d between the plates.

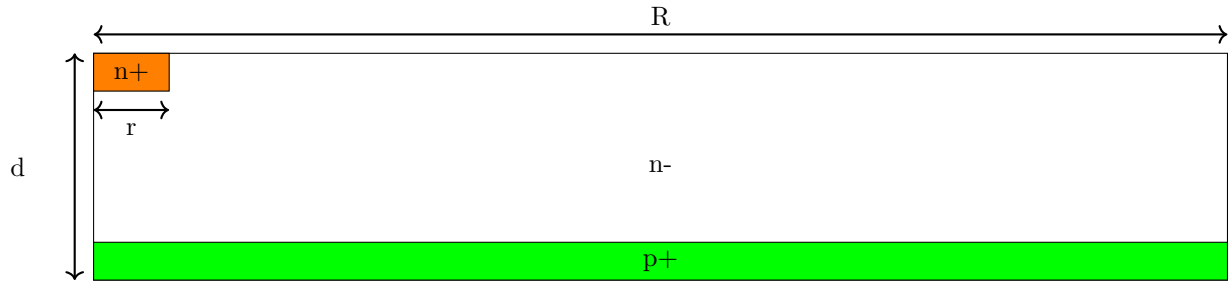


Figure 3.1: Structure considered for capacitance simulation

However, for small radius r, C is much larger than given by (3.1). This means C grows sub-quadratically so that at large r, C is given by (3.1) .

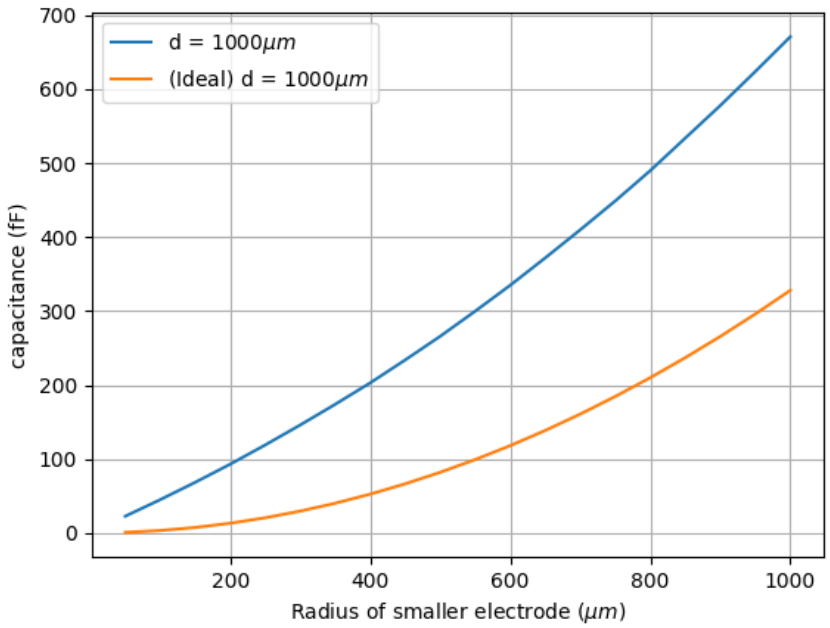


Figure 3.2: Real capacitance is much larger than given by (3.1) [$R = 5000\mu m$]

This can be also be seen as effective area being larger than area of anode because of fringing. Fringing effects becomes significant when actual area of the anode shrinks and becomes very low in comparison to d^2.

3.3 shows how effective area over which electric field lines spread has increased.As distance between electrodes decreases, fringing effects become smaller (see 3.4).

Expressing real capacitance in terms of $A_{effective}$,

$$C_{real} = \epsilon \frac{A_{effective}}{d}$$

Also,capacitance is relatively independent of R when $R/d >> 1$ (see 3.5). In large area SDDs, radius of detector is much larger than thickness of wafer. So, $R/d >> 1$ assumption is generally true.

Since $R/d >> 1$, capacitance should only depend on r and d. This means that effective area should only depend on ratio r/d. Taking fringing into account, there is a modified capacitance formula for a disk with radius r suspended a distance d above a ground plane [12] where $\frac{A_{effective}}{A_{anode}}$ is given by:

$$\frac{A_{effective}}{A_{anode}} = 1 + \frac{2}{\pi k_{Si}} \frac{d}{r} \left(ln \frac{r}{2d} + 1.41 k_{Si} + 1.77 + \frac{d}{r}(0.268 k_{Si} + 1.65) \right)$$

where k_{Si} is dielectric constant of Silicon

This formula improves the estimate for capacitance compared to ideal capacitance but it is still far from real capacitance. Better ans simpler estimate can be obtained for a small range of r and d by fitting the data (see 3.6).

Fitting leads to following simple form of A_{eff}.

$$A_{eff} = A_{anode}(k_1 \frac{d}{r} + k_2)$$

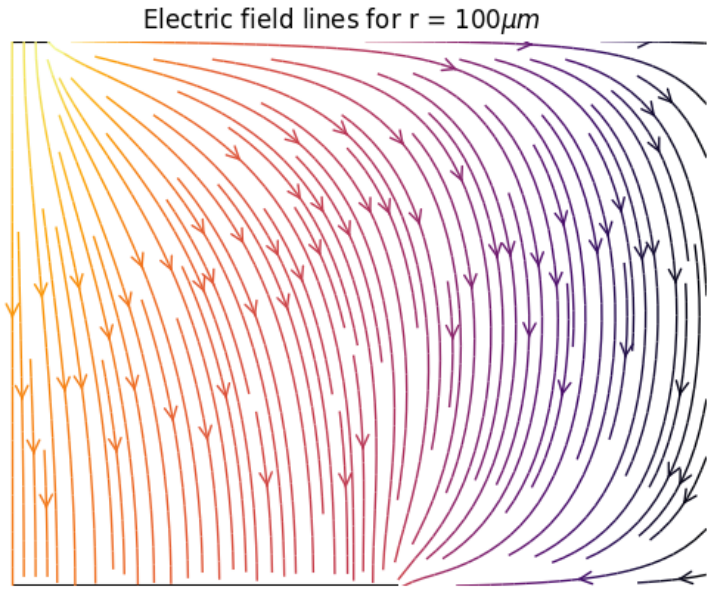


Figure 3.3: Fringing effect for capacitor with r = $100\mu m$. Highest electric field is at edge of top plate. (Left edge is the axis of rotation, Black borders at top and bottom show side view of electrodes)

where $k_1 = 1.32$ and $k_2 = 0.73$

Note that this is only accurate for small range of $r/d < 4$ as for large r/d A_eff should equal A_anode. In effect, the fit is just a linearisation of A_{eff}/A_{anode} curve for small range.

With these results, anode radius is chosen to be 100 μm and anode capacitance is 45 fF.

3.3 Structure

Substrate: n-Silicon with resistivity of $10k\Omega - cm$ is considered. This corresponds to donor density of about $5 \times 10^{11}/cm^3$. Low doping means lower depletion voltage.Depletion voltage for the structure is 380 V.
Doping: Magnitude of doping of $n+$ and $p+$ regions is set as $10^{18}/cm^3$.
Carrier lifetime: For leakage current, thermal generation should be low. So, SDD is manufactured using high-lifetime(¿1 ms) Si wafer So, SRH carrier recombination lifetime for both holes and electrons is set as $1ms$.
Carrier mobility: $\mu_n = 1000V - cm^2/s$, $\mu_p = 500V - cm^2/s$

3.7 shows the structure of SDD used for simulation. On top, n+ anode radius is 100 μm. Then,there is a voltage divider between two p+ strips determining surface potential.

The depth of high doped implants should be as low as possible. In simulation, depth of high doped regions is set as $1\mu m$. Thickness of polysilicon at the top is $1\mu m$.

Another structure was used for self biasing scheme.

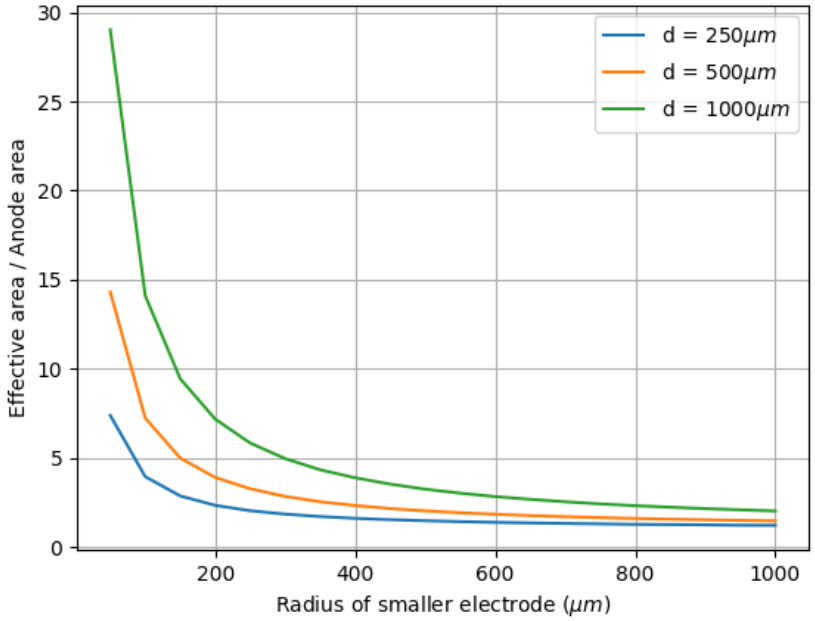


Figure 3.4: Effective area/Anode area increasing with decreasing central n+ electrode radius for different d

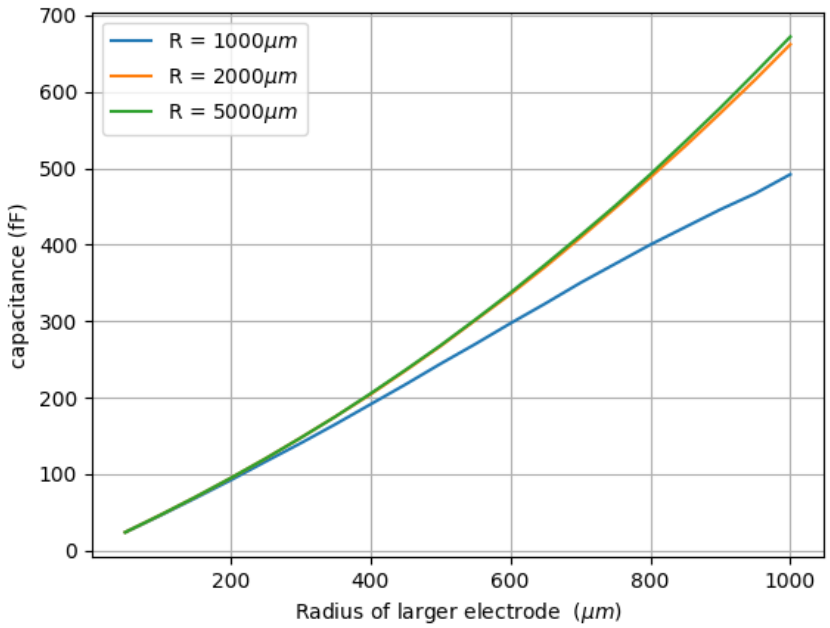


Figure 3.5: Capacitance is relatively independent of R while d is much smaller than R

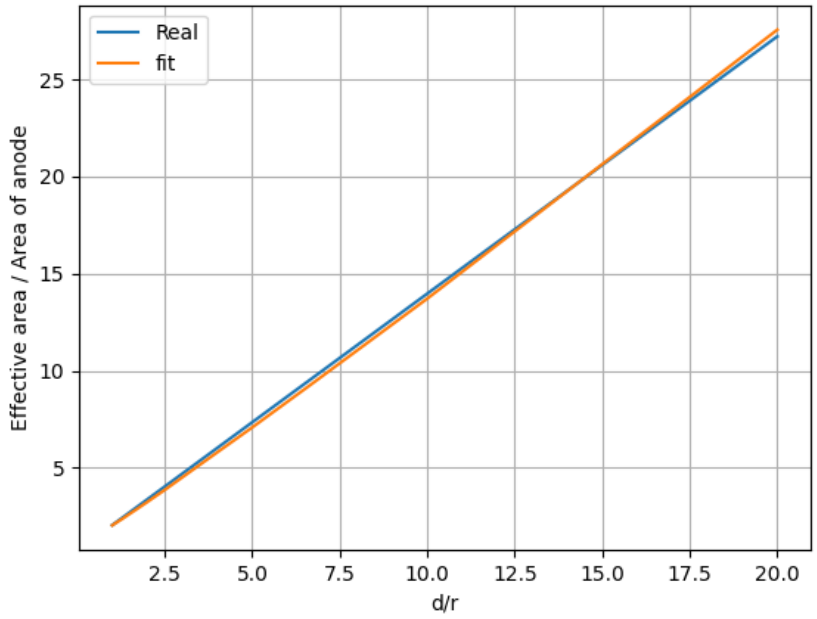


Figure 3.6: $\frac{A_{effective}}{A_{anode}}$ varies linearly with d/r

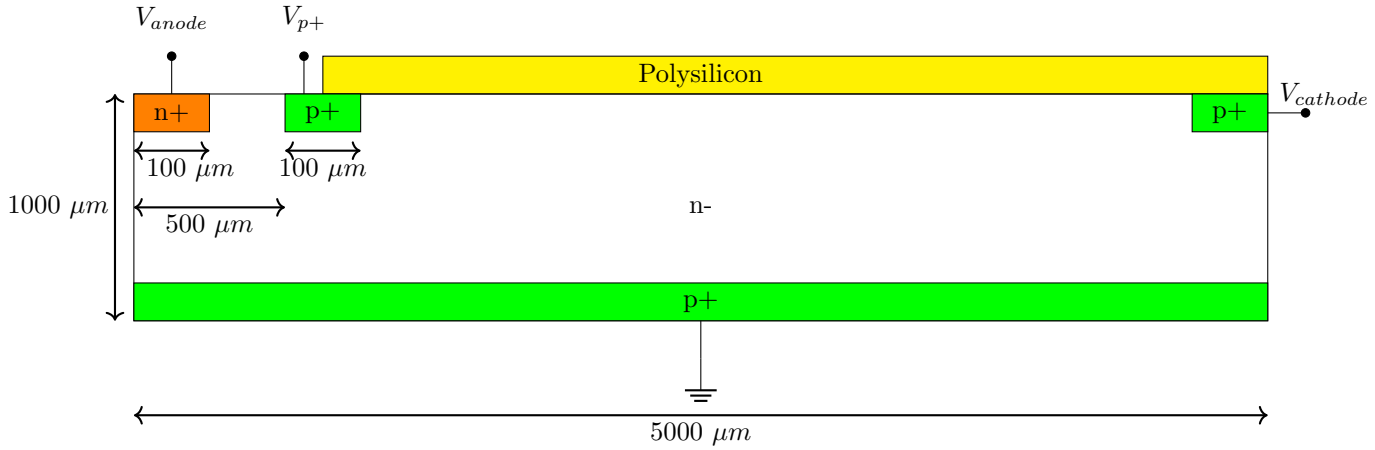


Figure 3.7: SDD structure considered for simulation (Left edge represent axis of cylindrical structure (r=0))

3.4 Designing Voltage divider

For designing the surface potential of the SDD, appropriate voltage divider needs to be designed with resistance per unit length deciding the surface potential profile.

Bulk resistivity of doped Si is given by:

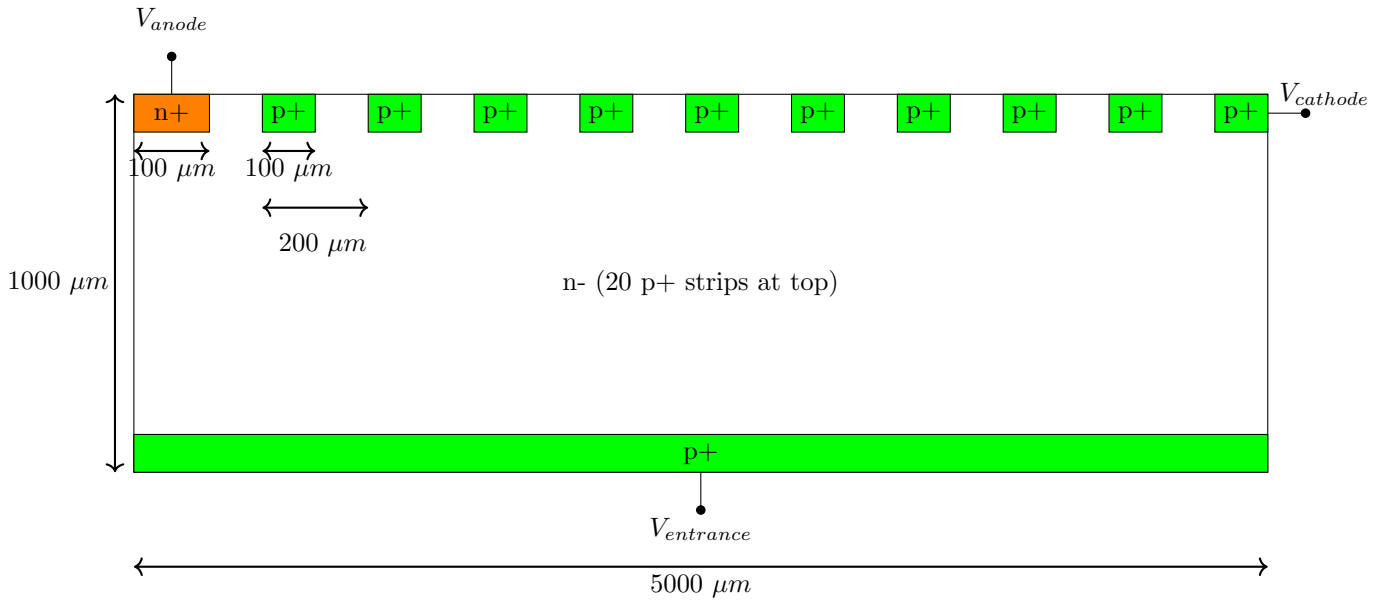


Figure 3.8: Self-biased SDD structure considered for simulation (there are 25 p+ strips at top and shallow p+ layer at the entrance)

$$\rho = \frac{1}{qN\mu_p}$$

where N is doping of p-doped poly-silicon

Sheet resistance of sheet of thickness t is given by:

$$R_{sheet} = \frac{\rho}{t} = \frac{1}{qN\mu_p t}$$

Then, resistance per unit width (R_{rad}) of annular disk of thickness t at radius r is given by:

$$R_{rad} = R_{sheet}\frac{w}{2\pi r}$$

From above discussion (see 3.10),it is clear that uniform doped layer cannot produce uniform resistance. To counter this, doping of p-doped layer needs to be decreased for outer p+ strips for uniform resistance. However, this is only true for annular disks.

In practice, rectangular poly silicon strips can be used as resistors connecting consecutive p+ strips. sFor rectangular strips of poly-silicon as resistors between strips, resistance per unit length in radial direction is given by:

$$R = \frac{R_{sh}}{width\ along\ the\ strip}$$

3.5 Leakage current

Bulk generation in fully depleted semiconductor is given by (1.5). Multiplying by detector volume and electronic charge, bulk generation is estimated.

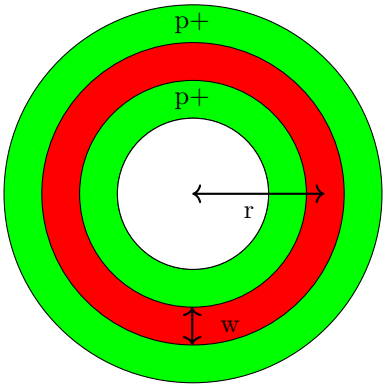


Figure 3.9: Red Annular disk showing resistor between two p+ strips

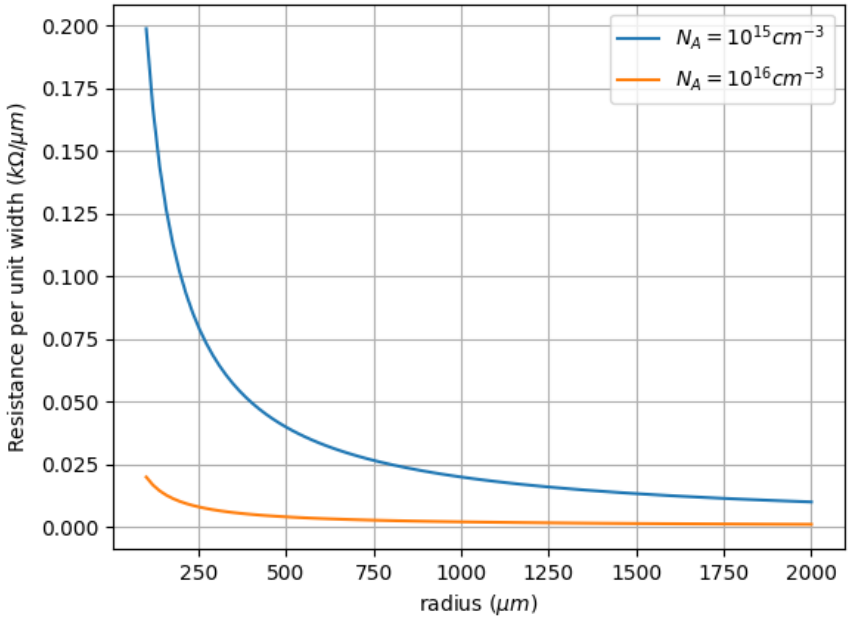


Figure 3.10: Resistance per unit width variation in radial direction for uniformly p-doped polysilicon sheet ($t = 1\mu m$)

For $\tau_n = \tau_p$=1 ms,

$$G = \frac{n_i}{\tau_n + \tau_p} = 1.5 \times 10^{10} \times 2 \times 10^{-3} cm^{-3} s^{-1} = 7.5 \times 10^{7} cm^{-3} s^{-1}$$

Detector volume(V) is given by:

$$R = 0.5cm$$
$$W = 0.1cm$$
$$V = \pi R^2 W = \pi \times (0.5)^2 \times 0.1 cm^3 = 7.85 \times 10^{-2} cm^3$$

Then, multiplying by detector volume, bulk generation current is given by:

$$I_{gen} = q \times G \times V = 1.6 \times 10^{-19} \times 7.5 \times 10^{7} \times 7.85 \times 10^{-2} = 94.2nA$$

So, bulk generation current is 94.2 nA for given structure and lifetimes. Doping at the contacts is high enough that diffusion current is much smaller than generation current (more than 3 orders of magnitude smaller).

So, in all the cases, anode leakage current is limited to the bulk generated current. Anode current equalling bulk generation current implies that all the thermal generated electrons are collected without recombination ensuring there is enough drift field for electrons generated at any point in the bulk to reach anode.

Initially, all electrodes are grounded and voltage on anode is increased which starts depleting SDD. Initially, as depletion region grows, anode current grows as $\sqrt{(V)}$ (see 3.11). At about 95 V ($\frac{1}{4}$ the PIN depletion voltage), SDD becomes fully depleted and anode leakage current saturates.

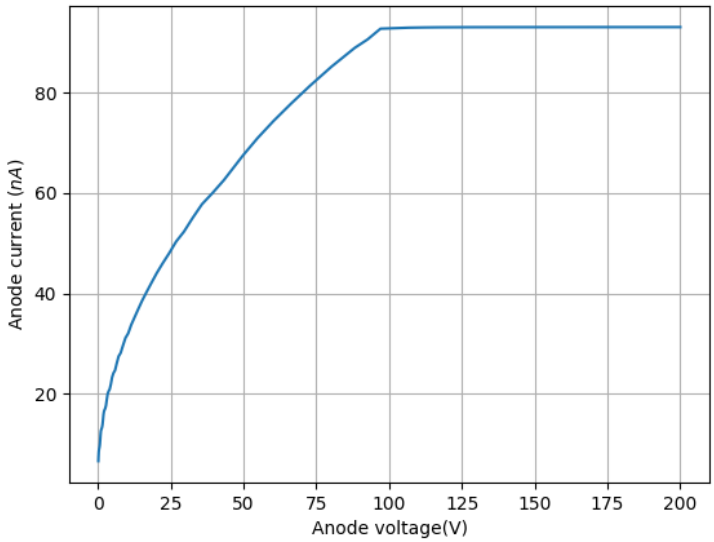


Figure 3.11: Anode leakage current

Further biasing changes do not change leakage current as SDD is fully depleted and thermal generation is at maximum.

3.6 Biasing and Surface potential

After depletion, top p+ strips are biased to create surface potential(radial electric field). Biasing of the p+ strips at the top needs to be done to avoid any breakdown.

Initially, following bias is applied.

$$\begin{aligned} V_{n+} &= 400V \\ V_{innerp+} &= 150V \\ V_{outerp+strip} &= -350V \\ V_{bottomp+} &= 0V \end{aligned}$$

At this bias, SDD is fully depleted.

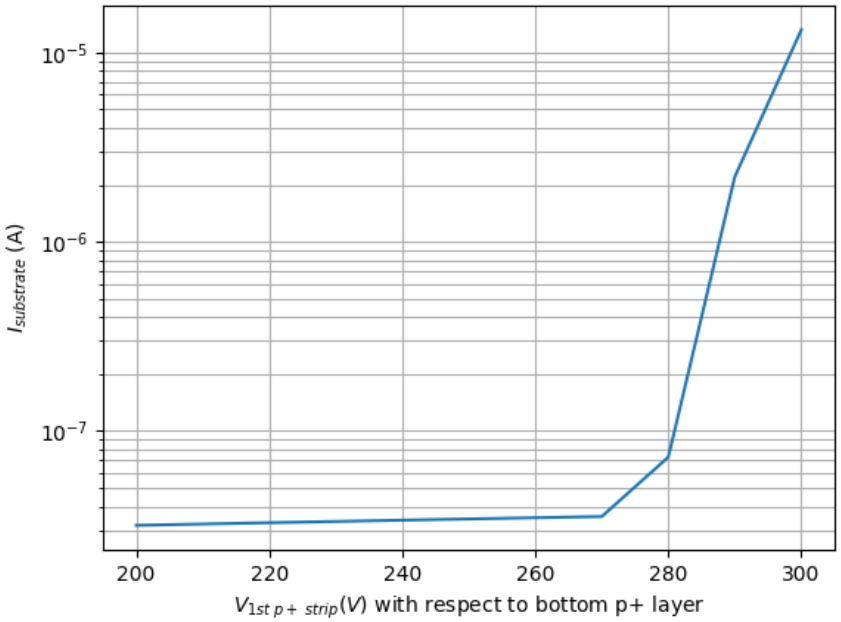


Figure 3.12: Punch through breakdown occuring at about 270 V difference between inner p+ strip and bottom p+ ($V_{dep} \approx 380V$) $[V_{n+} = 300V, V_{righttopp+strip} = -350V, V_{bottomp+} = 0V]$ for 3.7 with linear surface potential

Then the voltage bias on inner p+ is increased to find breakdown voltage.

3.12 shows substrate current suddenly increasing on increasing the voltage of inner p+ above 270 V. 3.13 shows sudden breakdown of depletion due to injection of holes from inner p+ on n-side.

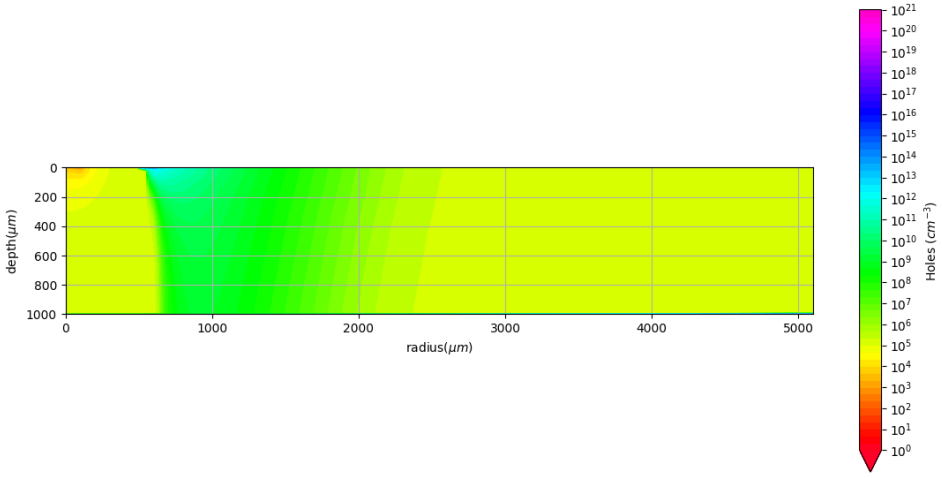
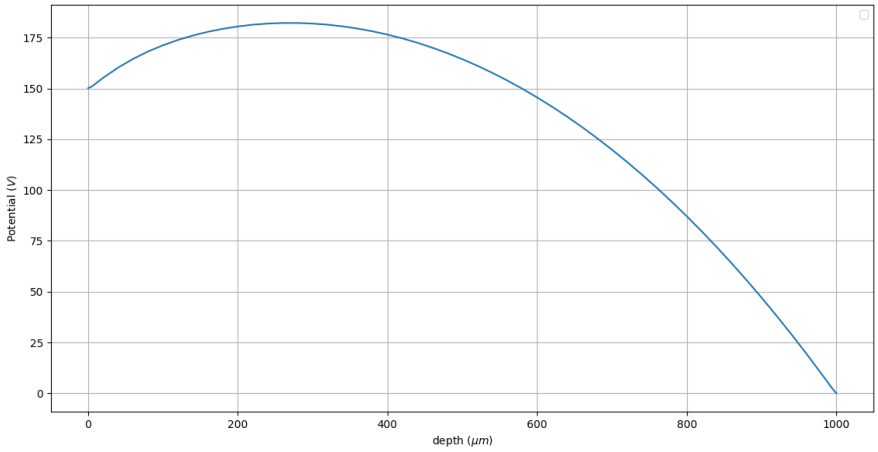
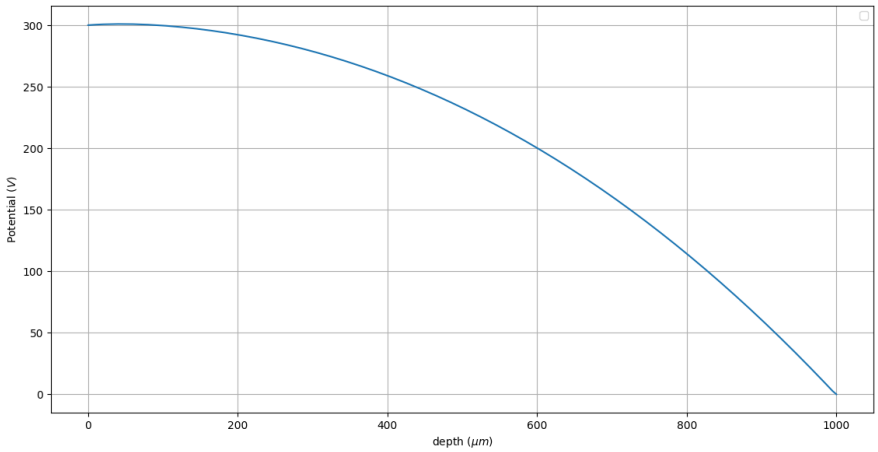


Figure 3.13: Holes being injected from inner p+ strip breaking down depletion (Voltage difference between top and bottom p+ is 300 V) in 3.7 with linear surface potential

So, the breakdown occurs due to punch-through phenomenon. Physically, even after full depletion,



(a) Before breakdown, there is a barrier of over 30 V when voltage difference between top and bottom p+ is 150 V. Potential diagram for 3.7 with linear surface potential at radius = 550 μm



(b) As voltage on top p+ is ramped barrier lowers and finally becomes small enough for holes to overcome.(voltage difference between top and bottom p+ is 300 V). Potential diagram for 3.7 with linear surface potential at radius = 550 μm

Figure 3.14: Potential barrier for hole between inner p+ strip and bottom p+

hole carrier density at p+ strips does not deplete and hole density in the p+ region is large compared to the bulk. But even though there is hole density difference, there is no injection of holes into the bulk due to a barrier of more than 30 V in the center as shown in 3.14a for holes to overcome (when voltage difference between the inner p+ strip and bottom p+ layer is 150 V). So, due to the large barrier, probability of overcoming the barrier is low. But, with increased bias, the barrier starts to shift towards the top p+ strip and also lowers in energy. At certain voltage , barrier height becomes small enough for holes to overcome and large number of holes are injected over the barrier from top p+ strip to the bulk where they are swept away by electric field towards the bottom p+. (see 3.14b).

It can be seen that punch-through breakdown occurs below the voltage difference of 380 V (which

is one dimensional PIN depletion voltage for same bulk doping). Similarly, holes are injected from bottom p+ to the top p+ layer when punch-through happens between them. Punch-through between outer p+ strip and substrate is found to be higher than 380 V. This is due to the breaking of our assumption earlier that radial field variation can be neglected.

Mathematically, for cylindrically symmetric system $\nabla.\vec{E}$ is given by:

$$\nabla.\vec{E} = \frac{1}{r}\frac{\partial(rE_r)}{\partial r} + \frac{\partial E_z}{\partial z} = \frac{E_r}{r} + \frac{\partial E_r}{\partial r} + \frac{\partial E_z}{\partial z} \tag{3.1}$$

where E_r and E_z are radial and vertical components of electric field respectively

In our one-dimensional analysis, we ignored contribution due to radial component (assumed $\frac{\partial(rE_r)}{\partial r} = 0$) of the electric field. For this assumption to be exact, E_r should be given by $\frac{f(z)}{r}$ for any function f. This means radial field should be decreasing with r. This is undesirable for any SDD. So, no SDD satisfies this condition.

3.15 shows barrier position by one-dimensional approximation((2.2)) and the solution obtained by two-dimensional simulation. It is seen that barrier is more closer to top side near inner p+ than given by (2.2) which leads tp lower breakdown voltage than depletion voltage. Similarly, barrier is farther than bottom p+ than given by (2.2) which increases the breakdown voltage.

This conclusion can also be derived from (3.1). There are two terms containing radial component of the field $\frac{E_r}{r}$ and $\frac{\partial E_r}{\partial r}$. $\frac{E_r}{r}$ is always positive since field is always radially outward. $\frac{\partial E_r}{\partial r}$ is positive near $r = 0$ as field is increasing near $r = 0$. This is always true as radial field at $r = 0$ is zero in cylindrically symmetric system and radial field is positive in bulk. So, $\frac{E_r}{r} + \frac{\partial E_r}{\partial r}$ is positive near 1st strip. So, $\frac{\partial E_z}{\partial z}$ under this condition is less than given by one-dimensional approximation under full depletion. So, vertical voltage that is possible under full depletion is lesser than depletion voltage.

Similarly, field also drops sharply near the right edge ($r = R$). So, $\frac{\partial E_r}{\partial r}$ is negative. Since E_r is very small near $r = R$ and r is large, $\frac{E_r}{r}$ is very small in magnitude compared to $\frac{\partial E_r}{\partial r}$ and contribution of radial terms is negative(see 3.16). So, vertical voltage that can be sustained is greater than depletion voltage.

Physically, what this means is atomic dipoles of donor ions are not aligned completely vertical which actually leads to variation in radial electric flux. So, vertical voltage range possible in SDD is different from predicted by one-dimensional analysis.

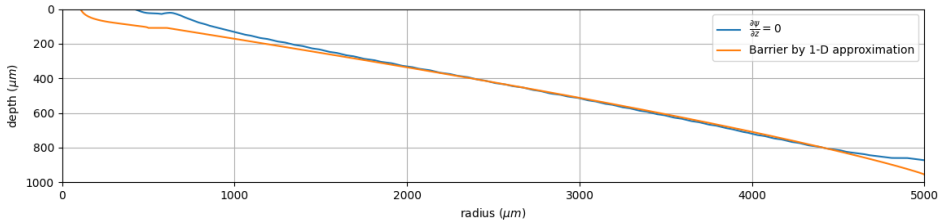


Figure 3.15: Potential barrier position is more closer to the inner p+ than barrier position given by (2.2).Potential barrier position is farther from bottom p+ layer than barrier position given by (2.2).Barrier position calculated for 3.7 with linear surface potential when breakdown occurs near inner p+.[$V_{n+} = 300V, V_{righttopp+strip} = -350V, V_{bottomp+} = 0V$]

Taking the breakdown voltage into account, following bias voltages were set for both the cases.

$$\begin{aligned} V_{anode} &= 300V \\ V_{cathode} &= -400V \\ V_{p+} &= 250V \\ V_{bottom} &= 0V \end{aligned}$$

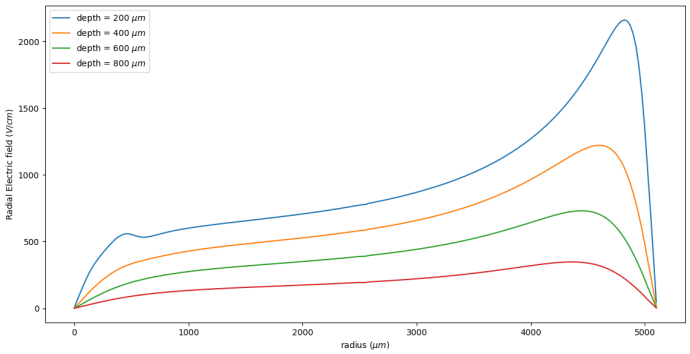


Figure 3.16: Radial field variation for 3.7 with linear surface potential $[V_{anode} = 300V, V_{cathode} = -400V, V_{p+} = 250V, V_{bottom} = 0V]$

Surface potential	Current (mA)	Total Resistance ($k\Omega$)	Power(W)
Straight	34.2	19	22.23
Curved	8.79	74	5.7

Table 3.1: Chain current and power consumption

Considering the above structure and biasing, two different surface potentials are designed using top voltage divider.

Resistance distribution of the top voltage divider was such that it led to a straight line potential(see 3.17,varies linearly with r) and a curved surface potential (see 3.18) very close to the optimum surface potential(varies as $\sqrt{1 - r/R}$ with r) derived later(see 3.23).

Poly-silicon resistance per unit width for curved surface potential is 50 $\Omega/\mu m$ and for straight line potential is 20 $\Omega/\mu m$. Lower resistance leads to straight surface potential while higher resistance leads to curved surface potential. When resistance is low, chain current is high and current contribution from bulk does not determine the surface potential but for higher resistance the chain current is lower and current contribution from bulk also determines the surface potential.

So, one possibility is to have complete self biasing of the strips. Self biasing is done in 3.8.

For self-biased structure, following are the applied bias. In self-biased structure, only anode, cathode and bottom electrode are biased.

$$V_{anode} = 350V$$
$$V_{cathode} = -400V$$
$$V_{bottom} = 0V$$

3.6.1 Resistor Chain Current and Power Consumption

3.1 lists chain current and power consumption for both surface potentials.

As discussed earlier, mean radial drift field needs to be increased in order to decrease drift time. So, it is necessary to set bias potentials on p-side surface such that radial drift field set up in the cylindrical SDD is optimum.

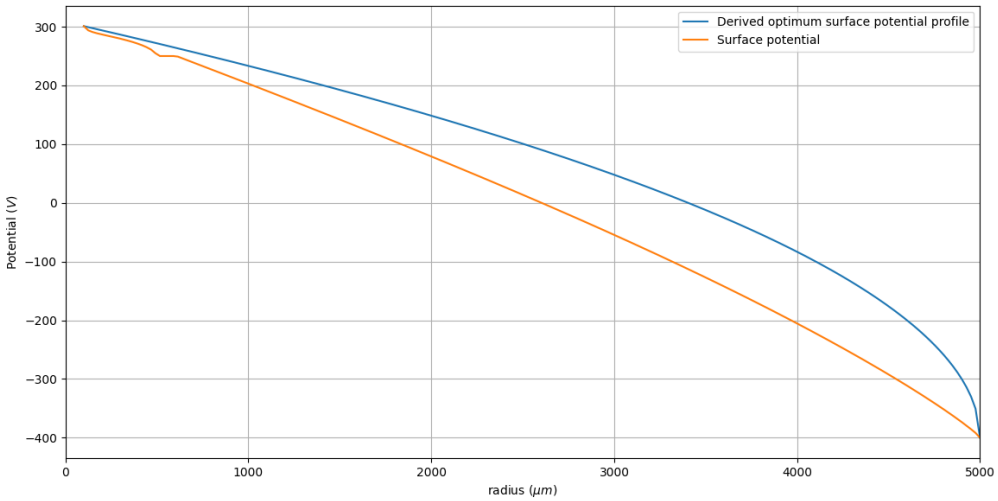


Figure 3.17: Linear surface potential

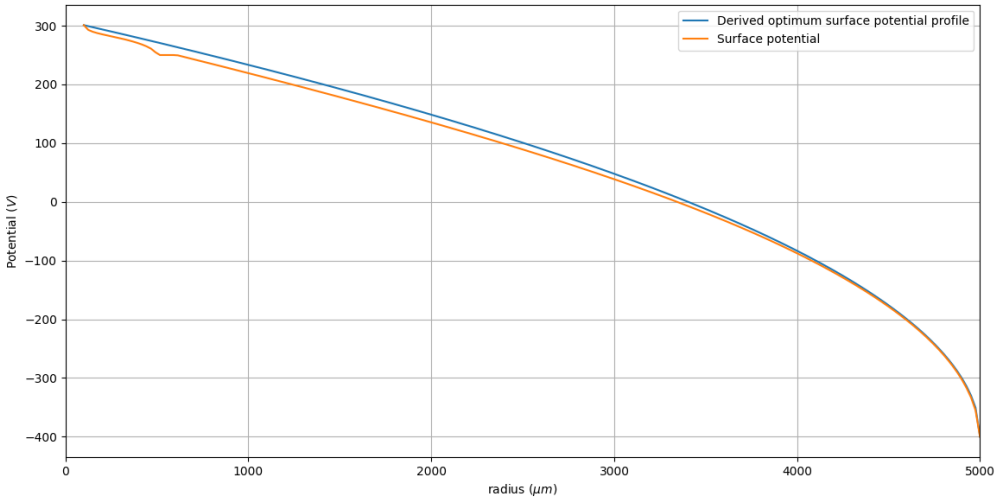


Figure 3.18: Curved surface potential

3.6.2 Drift channel

In SDD of chapter 1, it was observed that there forms a electron potential valley in center of the detector with one p+ layer at the top. Electrons accumulate in the valley and drift towards the anode due to electric field.

When the top p+ layer is divided into strips applying increasing electron potential from inner p+ strips to outer p+ strips, the distance of electron potential valley from p+ strips increases with increasing radius. Generated electrons experience a strong electric force towards the valley and quickly move to the valley. Then, they drift along the valley towards the anode since the electric field in the

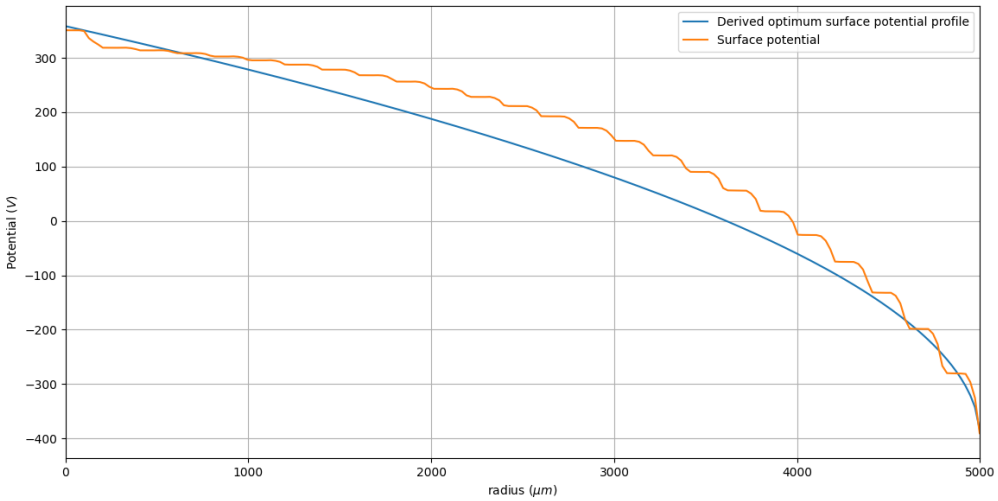


Figure 3.19: Self-biased surface potential

valley is always along the valley. This is the defining property of drift channel.

Let $z(r)$ be the distance z from top p-side at radius r along an electric field line. Then, by definition, electric field at any point on curve $z(r)$ should be tangential to it.

$$\frac{d}{dr}z(r) = \frac{E_{drift,z}}{E_{drift,r}}$$

It is seen that electrons accumulate along a curve in the SDD. The region of high electron density can be computed by computing position of electron density maxima at a particular radius r and can be defined by :

$$\left(\frac{\partial n}{\partial z}\right)_{z=z(r)} = 0$$

The locus of critical points lie along an electric field line as any electric field perpendicular to it would distort the shape of locus. So, this serves as drift channel definition in this thesis.

3.6.3 Drift field along drift channel

In semiconductors, under the model that velocity of charge carrier is parallel to electric field (neglecting diffusion), charge carriers always move along a particular electric field line after generation. So, electric field line from the point of generation to anode is the trajectory of generated electron cloud electron (neglecting diffusion).

Drift field outside the drift channel is significantly larger compared to electric field along the channel. So, generated electrons move quickly towards the drift channel and the time taken to reach the channel is small compared to total drift time.

This above arguments justify the reasoning for choosing this definition.

So, only (radial) drift field along the channel is considered here for mean (radial) drift field estimation.

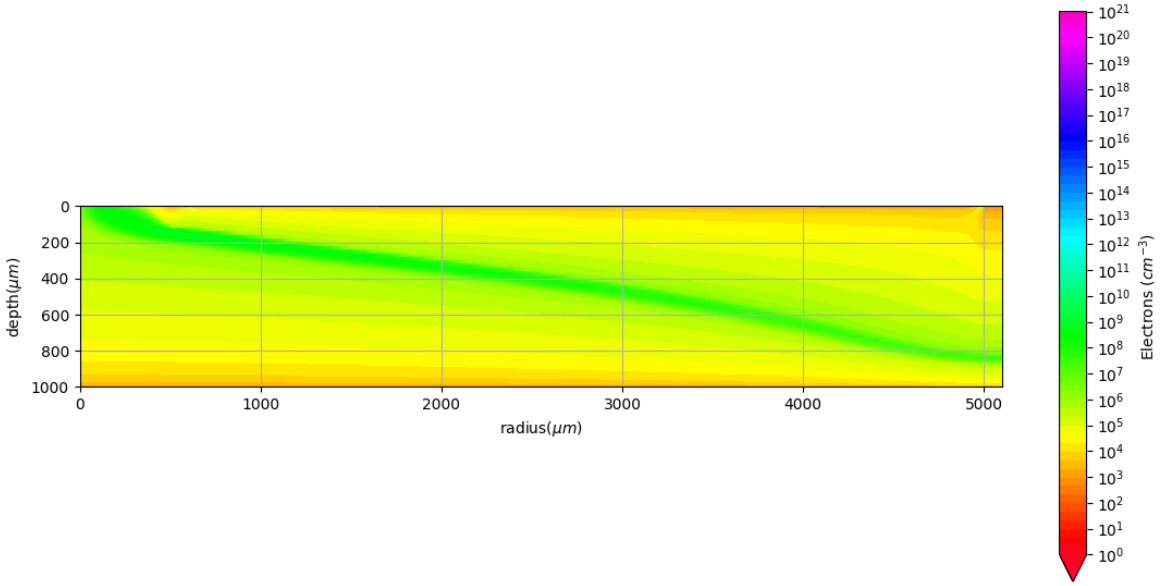


Figure 3.20: Electron density is much higher in the channel than in depleted bulk.

$$E_{drift,mean} = \frac{r - r_0}{\int_{r_0}^{r} \frac{dr}{E_{drift,r}}}$$

So, mean drift field along drift channel determines the drift time. As noted earlier, low electric field region along the channel proves to be bottleneck and influence mean drift field strongly. So, the goal of detector design is to ensure uniformity in drift field along the channel.

3.21 shows electric field lines over electron density contour plot. The figure shows that maximum electron density lies along an electric field line and electric field lines diverge away from it as they move away from anode. So, for electrons, after generation, their path quickly converges to the drift channel.

3.6.4 Optimum drift field

This section discusses the optimum drift calculation done by [13] in their paper titled Spiral drift detectors. Potential throughout this section means electron potential (negative potential).

Assuming potential varies very quickly along vertical dimension compared to radial dimension, 2-D poisson equation is approximated by 1-D poisson equation as:

$$\nabla^2\psi \approx \frac{\partial^2\psi}{\partial z^2} = \frac{qN_D}{\epsilon}$$

where ψ defines electron potential

$$V_{dep} = \frac{qN_D d^2}{2\epsilon}$$

where V_{dep} defines depletion voltage

To define boundary conditions at a particular radius r, potential at p-side is assumed to be constant while potential at n-side is given by function ϕ_r. Goal is to find optimum surface potential(ϕ_r) for

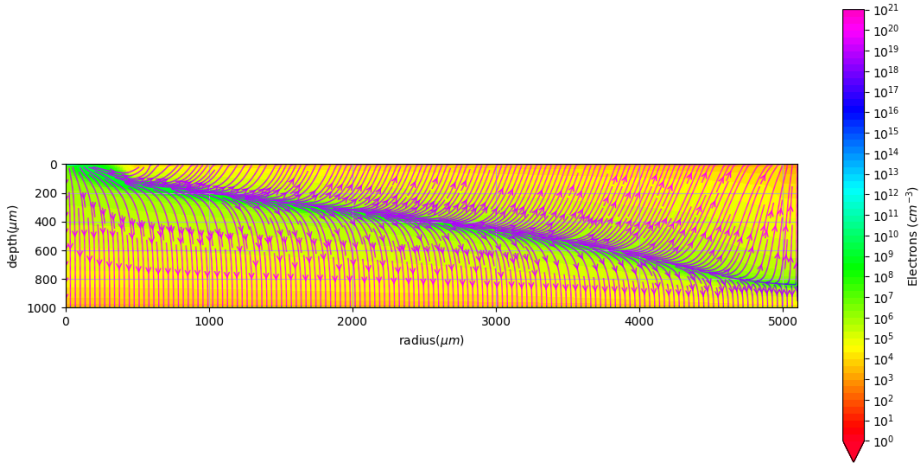


Figure 3.21: Electric field lines starting from anode diverging away from channel (Electric field lines over electron density contour plot)

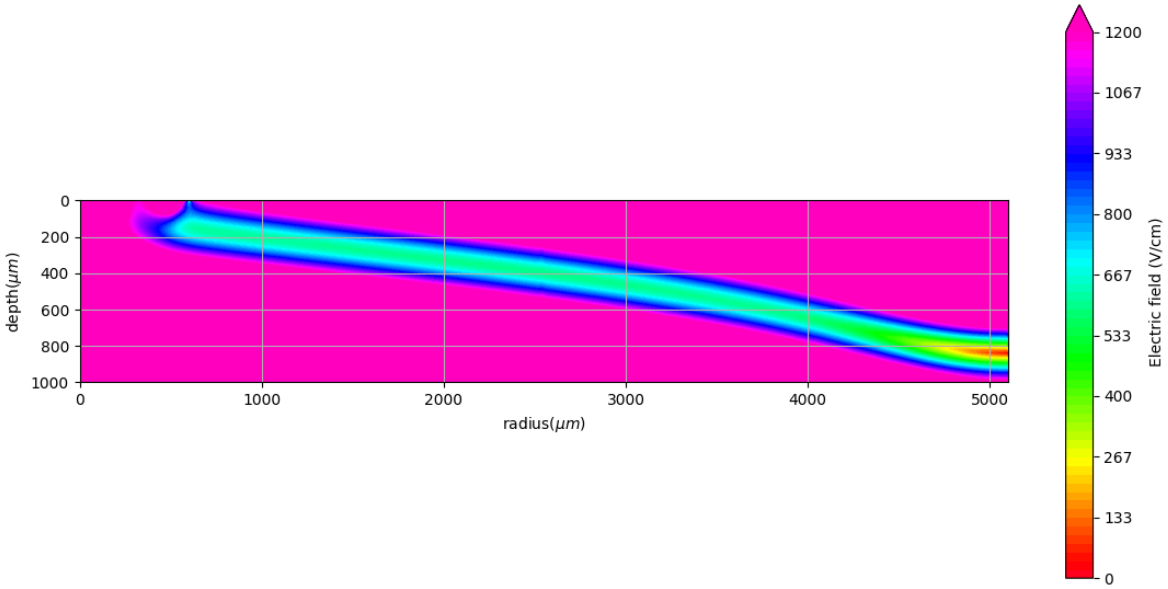


Figure 3.22: Electric field is much higher in the bulk compared to the channel

maximum radial drift field.

For maximum drift field, surface field should be as high as possible which means highest possible (negative) voltage on the outermost electrode. Punch-through breakdown puts constraints on maximum (negative) biasing voltage on n-side. So, maximum biasing voltage possible on n-side is $2V_{dep}$ when voltage on p-side is fixed to V_{dep}. So, potential on p-side is fixed to V_{dep}.

With these boundary conditions, solution for potential is given by :

$$\psi(r,z) = V_{dep}\left(\frac{z}{d}\right)^2 + \phi(r)\left(1-\frac{z}{d}\right)$$

Then, potential minimum $\psi_{min}(r)$ at radius r is calculated. It is at distance $z_{dr}(r)$ from top p-side given by

$$z_{dr}(r) = \frac{d}{2}\frac{\phi(r)}{V_{dep}}$$

Then, potential minimum $\psi_{min}(r)$ at radius r is given by

$$\psi_{min}(r) = \psi(r, z_{dr}(r)) = \phi(r)\left(1-\frac{\phi(r)}{4V_{dep}}\right)$$

Here, since drift field is assumed to be radial (vertical field is neglected), $E_{drift,r} \approx \frac{d\psi_{min}}{dr}$ along the drift path.

$$\implies E_{drift,r} \approx \frac{d\psi_{min}}{dr} = \phi'(r)\left(1-\frac{\phi(r)}{2V_{dep}}\right) \qquad \left[\phi'(r) = \frac{d\phi}{dr}\right]$$

Then, the radial drift field along the drift path $z_{dr}(r)$ is calculated and drift time is integrated from radius r_0 to r.

$$t = \int_{r_0}^{r} \frac{1}{\mu}\frac{dr}{E_{drift,r}} \approx \frac{1}{\mu}\int_{r_0}^{r}\frac{dr}{\frac{d\psi_{min}}{dr}}$$

So, $\frac{1}{E_{drift,r}}$ is a function of $\phi(r)$ and $\phi'(r)$ which can be written as $L(\phi(r), \phi'(r))$ for some function L.

$$t = \frac{1}{\mu}\int_{r_0}^{r} L(\phi(r), \phi'(r))$$

Then,$\phi(r)$ for which t is minimised is given by Euler-Lagrange equation.

$$\frac{\partial L}{\partial \phi} = \frac{d}{dr}\frac{\partial L}{\partial \phi'}$$

So, given boundary conditions, Euler-Lagrange equation gives optimum solution.
Setting $\phi(R) = 2V_{dep}$ and $\phi(0) = 0$, optimum $\phi(r)$ and $z_{dr}(r)$ is given by

$$\phi(r) = 2V_{dep}\left(1-\sqrt{1-\frac{r}{R}}\right)$$

$$z_{dr}(r) = d\left(1-\sqrt{1-\frac{r}{R}}\right)$$

$$\implies E_{surface,r} = \frac{d}{dr}\phi(r) = \frac{V_{dep}}{R}\frac{1}{\sqrt{1-\frac{r}{R}}}$$

Then, optimum radial drift field along the channel is given by:

$$E_{drift} = \frac{V_{bottom}}{R}$$

This optimum drift path has uniform radial drift field as expected.

Optimum solution leads to a curved drift channel starting from anode and curving towards bottom electrode at a diverging rate. This leads to the stringent requirement of $E_{surface,r}$ radial surface field to also diverge with increasing radius (see 3.23). So, radial electric field in all cases will drop near the outer side of detector. Channel is farthest from top side near the outer radius and bottom p+ layer is fixed at a constant potential (zero radial field). So, radial electric field at the top near the edge has very small effect at the channel. This reasoning also makes it clear that radial electric field at the top needs to be increased moving outwards as channel moves away from top p-side.

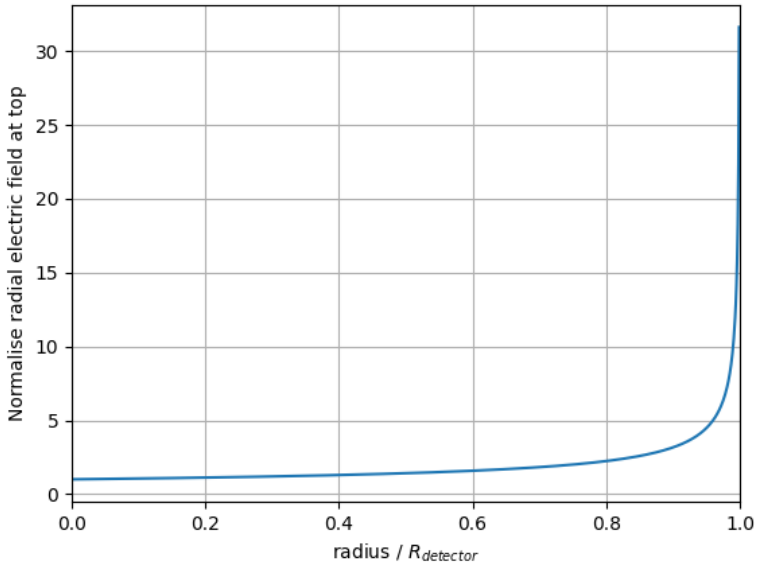


Figure 3.23: Surface electric field leading to curved optimum drift channel

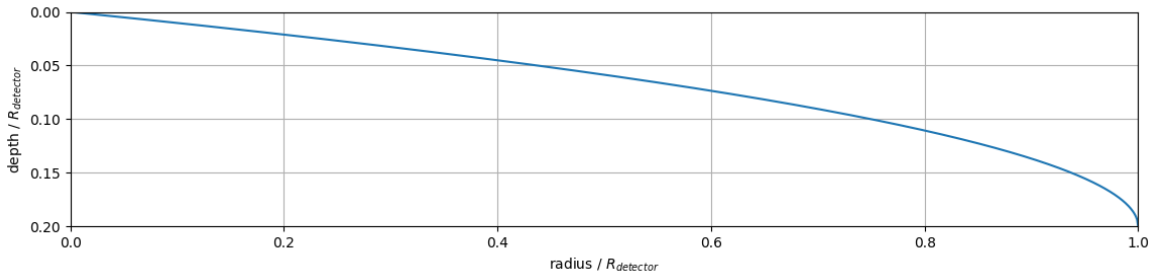


Figure 3.24: Optimum curved drift channel

Drift path used in this derivation here has zero electric field in vertical dimension. This approximation is only justified when vertical length of drift path is much smaller than radial length and would

give appropriate drift time only if thickness is much less than radius (making drift field almost equal to drift field). The drift channel considered in this thesis is appropriate for all aspect ratios.

Here,for the detector considered, $R = 5mm$ and $d = 1mm$ which means $\frac{R}{d} = 5 >> 1$ and there is not much difference between both definitions. The drift channel defined here is shifted just a bit (see 3.25) towards p-side with respect to drift path defined by [13].

Note here that radial drift field is actually limited by potential difference between bottom p-layer and n+ anode. Drift channel starts near bottom p-side and ends at the anode. So, potential difference across two ends of drift channel is about potential difference between bottom p-layer and n+ anode. So, maximum mean drift field possible is

$$E_{drift,max} = \frac{V_{anode} - V_{bottom}}{R}$$

Derived optimum path achieves this. So, to prove optimality of surface potential profile, one needs to show that mean drift field is close to maximum drift field possible.

3.6.5 Simulation

Using the above concepts of drift channel and drift field, the drift channel and drift field are calculated along the drift channel for both the surface potentials.

3.25 shows drift channels for different surface potentials. As expected, curved and straight line potential lead to curved and straight line channels.

For comparison, definition of drift path used by ($\frac{\partial \psi}{\partial z} = 0$) [13] is also shown which demonstrates that there is little difference between two definitions for large R/d.

3.26 shows potential along the drift channel for different surface potentials. Potential range is limited by voltage difference between anode and bottom p+.

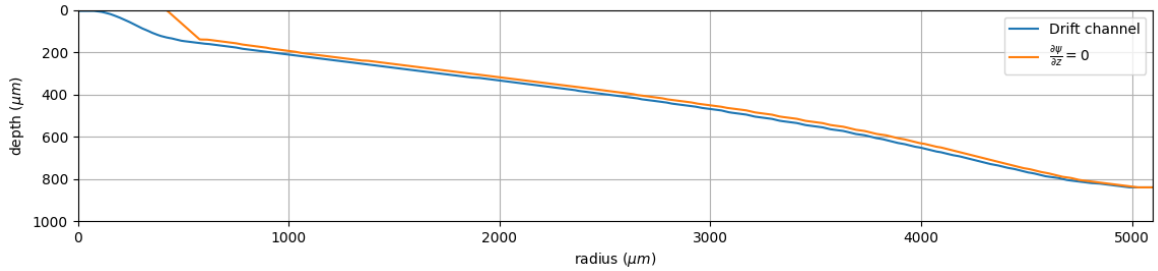
3.27 shows potential along the drift channel for different surface potentials. As expected, radial drift continuously decreases moving outwards for effect of constant surface field diminishes as channel moves further away from top surface. Similarly, for self-biased potential, radial field is lower for smaller radius and peaks near the outer edge and decreases sharply again outwards. This clearly shows that optimum surface potential should be between self biased and straight line potential.

These effects are properly balanced out by curved optimum surface potential by providing increasing surface field. Though it can be still seen that at outer edge field decreases. This is expected as for uniform radial field, the surface field requirement becomes very stringent (see 3.23) near the outer edge.

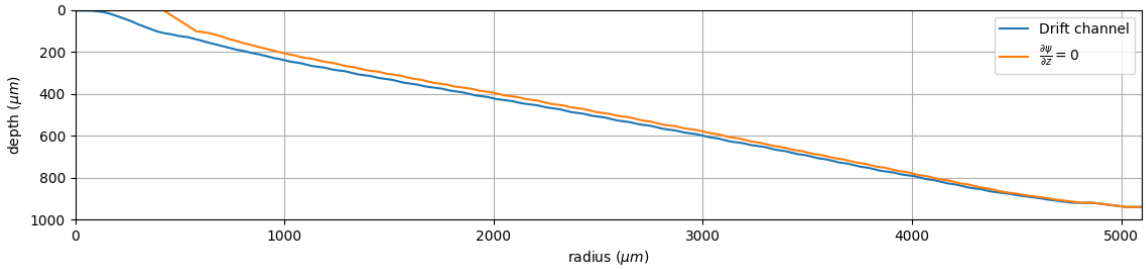
In further sections, since self-biased structure is found to be sub optimal, only comparison between linear surface potential and curved surface potential is discussed.

3.7 Anode Capacitance of designed SDD (with voltage divider)

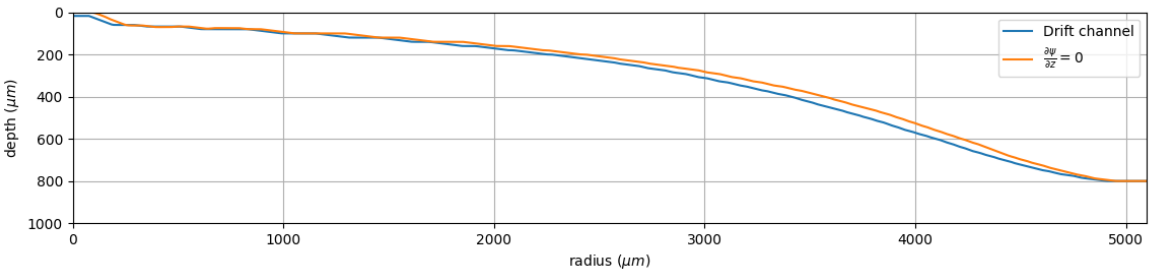
Anode capacitance saturates to low value of about 48 fF at full depletion. Anode capacitance here refers to capacitance of n+ electrode with respect to ground. Since geometry of structure (position and dimensions of electrodes) is same for both surface potentials, capacitance for both cases are equal. 3.2 shows mutual capacitance between anode and other electrodes for structure with poly-Si on top.



(a) Curved surface potential leading to curved drift channel



(b) Linear surface potential leading to straight drift channel



(c) Self-biased surface potential leading to curviest drift channel

Figure 3.25: Drift channel for different surface potentials

3.8 Transient Response

3.8.1 Drift time along the channel

Drift time along the channel is given by 1.4 defined in chapter 2. Numerical integration of drift along the channel can give good estimate of drift time.

$$t = \int_{r_0}^{r} \frac{dr}{\mu_n \; E_{drift,r}}$$

where r_0 is the radius of anode and r is radius of point of generation

3.8.2 Interpretation using Schokley-Ramo Theorem

For the electron trajectory along the drift channel, one can calculate induced current using Schokley-Ramo Theorem (neglecting diffusion).

Electrode	Mutual Capacitance between anode and electrode (fF)
Bottom p+	13.1
Inner p+	33.3
Cathode	1.59

Table 3.2: Mutual capacitance between anode and other electrodes

$$I_{induced} = nq\ \vec{v}.\vec{E_0} = nq\ \mu\vec{E}_{drift}.\vec{E}_0$$

where n is number of generated electrons,$\vec{E}_{drift}$ is drift field along the channel and $\vec{E}_0$ is weighing field.

So, to estimate induced current on anode, weighing potential and weighing field are calculated for anode in the introduced SDD structure. The weighing potential(ϕ) is a solution of Laplace equation with boundary conditions such that anode is at unit potential and other electrodes are grounded.

The weighing potential is calculated for structure with voltage divider on top.

$$\nabla^2\phi = 0$$
$$\phi(anode) = 1, \phi(p+\ \ strips) = \phi(bottom\ p + layer) = 0$$

Assuming complete collection, actual peak current would be less than predicted by Schokley-Ramo theorem since the peak broadens due to diffusion.

3.28 shows weighing potential for the SDD described above.

Weighing potential changes very slowly far away from the anode resulting in low weighing field in the bulk but changes very quickly near the anode. So, weighing field is very high near the anode. This has two consequences:

- Induced current changes very slowly for movement of carriers far way from anode. Induced current peak occurs when the electron is near the anode. So, electron drift time can be estimated by observing the current peaking time.
- Since holes move towards p+ strips from the point of generation, the weighing potential change for holes is very small from point of generation to the point of collection unless they are generated very near the anode. So, induced current on anode is mainly due to movement of electrons. Hence, induced current can be estimated by drift of electrons along the drift channel.

  This is different from PIN diodes. For PIN diode where both electrodes are equal in size, weighing potential is linear between the two electrodes where weighing potential is 1 at electrode of interest and zero at the other electrode which means weighing field is constant and equal to $\frac{1}{d}$ where d is the distance between electrodes. So, induced current only depends on distance between the electrodes and electric field in the diode. So, both carriers contribute to the current on each electrode.

3.8.3 Simulation

A triangular pulse of width $0.1ns$ is incident at different radial distance from anode in the SDD . Transient response at anode is solved using poisson equation and continuity equations. Then, induced anode current is calculated subtracting background leakage current.

Induced anode current is given by:

$$I_{induced} = I - I_{leakage}$$

Drift distance (μm)	$\frac{I_{peak}}{Generated\ charge}(\mu s^{-1})$	Drift time [t_0] (ns)	$\sigma(ns)$
1500	16.0	179	24.8
2500	12.2	317	33.4
3500	8.99	497	46.6
4500	5.33	851	74.5

(a) Linear surface potential

Drift distance (μm)	$\frac{I_{peak}}{Generated\ charge}(\mu s^{-1})$	Drift time [t_0] (ns)	$\sigma(ns)$
1500	12.3	230	27.2
2500	9.3	400	37.3
3500	7.77	569	5.11
4500	6.72	745	52.4

(b) Curved surface potential

Table 3.3: Parameters of Gaussian fit to induced anode current

Total charge collected can be estimated by:

$$Q = \int_0^{\delta t} I_{induced} dt$$

where δt is width of the transient response.

Charge collection efficiency is given by:

$$\eta = \frac{Q}{Q_{generation}} = \int_0^{t_0} \frac{I_{induced}}{Q_{generation}} dt$$

Integrating over the induced anode current per unit generated charge gives collection efficiency

In the following figures, induced anode current per unit generated charge is plotted. So, area under the plot is the collection efficiency of the structure.

From 3.30, it can be seen that pulse is symmetric about the peak. Since diffusion is the broadening process for electron cloud, the collection time (drift time) broadening takes form of a gaussian distrbution. So, gaussian fits well to the induced current-time profile. Various gaussian parameters for the transient response are shown in 3.3b.

$$I_{induced} = I_{peak} e^{\frac{(t-t_0)^2}{2\sigma^2}}$$

As drift distance increases, σ increases due to diffusion as explained earlier. But since collection efficiency (≈ 1) is constant, I_{peak} decreases. This shows that, for same amount of charge, induced current decreases with increasing radius at the point of generation. For correct charge estimation, induced current should be significantly higher than shot noise due to leakage current.

As signal spread increases with drift time, this is limited by maximum drift time given by $\frac{R_{detector}}{E_{drift}}$.

Collection efficiency was found to be above 99 percent for all cases with very small variance.

Curved surface potential leads to linear relationship between drift time and drift distance as expected from uniform radial drift field. Straight line potential has lower drift times than curved surface potential for small drift distance due to higher field near the anode but decreasing radial field outwards leads to super-linear increase in drift time.

So, optimum surface potential enables good radial position sensing due to drift time-distance linearity.

Surface potential	Mean drift field [V/cm] (extracted from transient response)	Mean drift field [V/cm] (by integration)
Curved	604	598
Straight	529	531

Table 3.4: Mean drift field comparison

Mean drift field can be extracted from transients by dividing maximum drift distance by drift time and electron mobility. 3.4 shows comparison between estimation of mean drift field using two methods.

From 3.29 and 3.4, validity of drift time calculation along the drift channel is demonstrated.

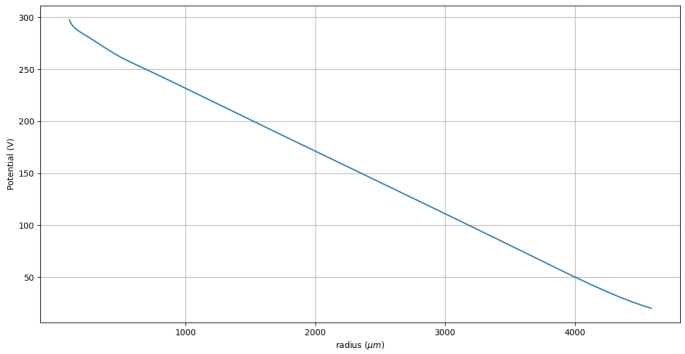
Maximum mean drift field possible for the given biasing is:

$$E_{drift,max} = \frac{V_{anode} - V_{bottom}}{R} = 600V/cm$$

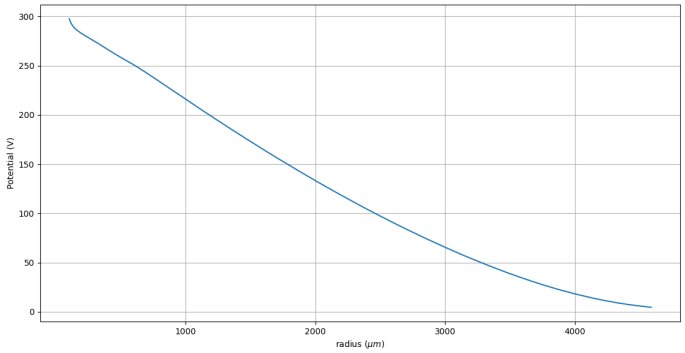
This shows that curved surface potential is optimum.

One final point to note is that calculations were done for $r = 4500\mu m$. If we calculate mean drift field for $r = 4750\mu m$, mean drift field drops to 557 V/cm and 417 V/cm for curved surface potential and straight surface potential. This is expected as channel gets very close bottom p+ layer.

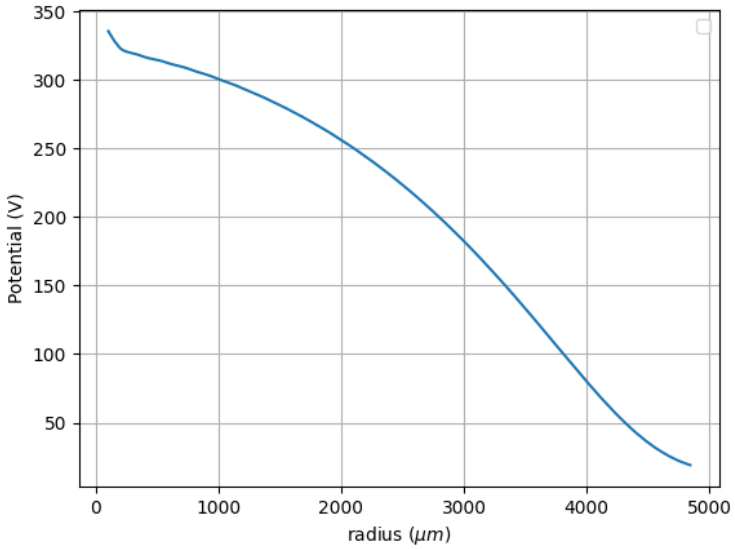
Still, the electric field drop in optimum surface potential is within acceptable limits.



(a) Curved surface potential

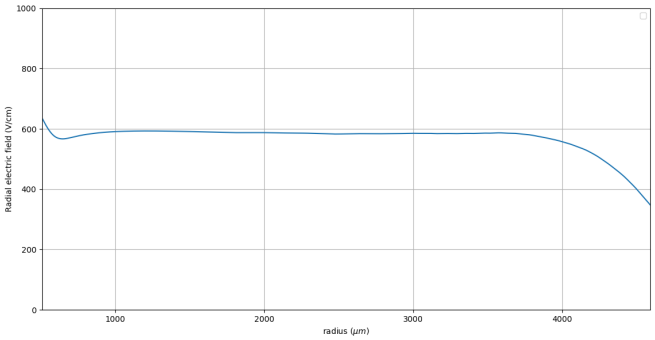


(b) Linear surface potential

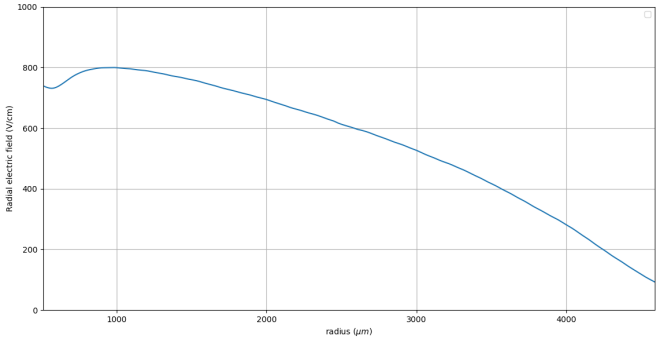


(c) Self biased

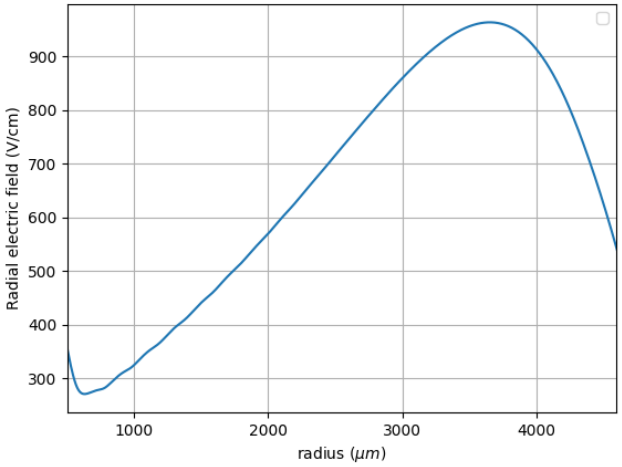
Figure 3.26: Potential along drift channel for different surface potentials



(a) Curved surface potential

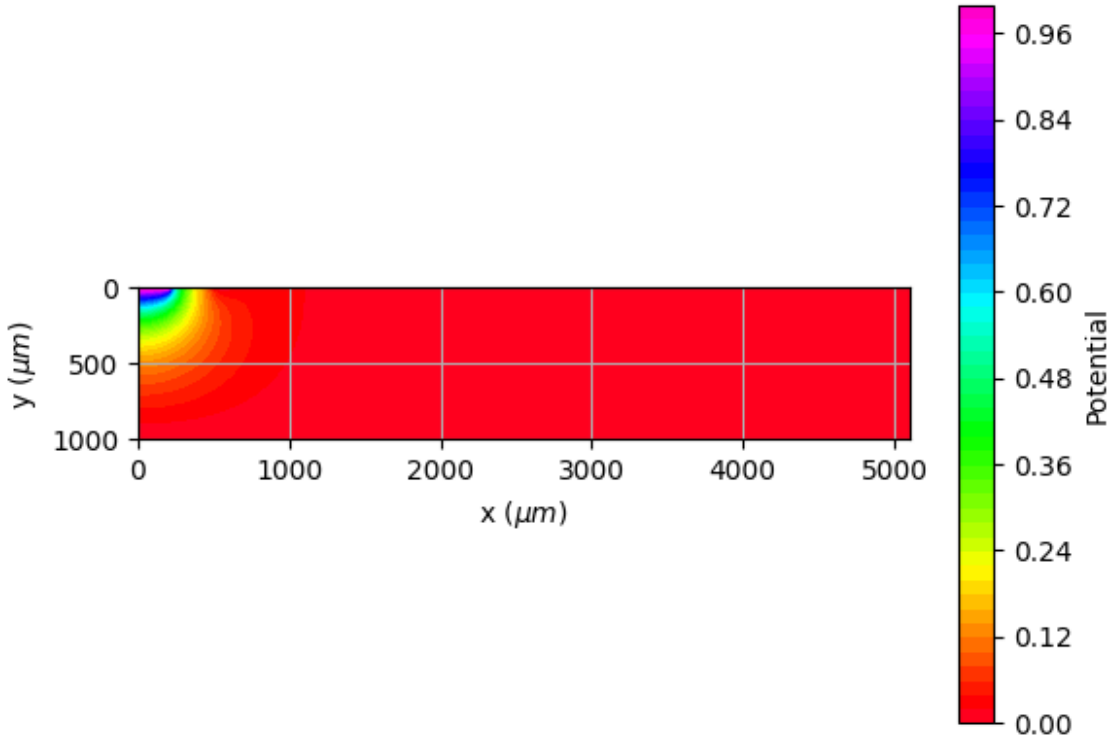


(b) Linear surface potential

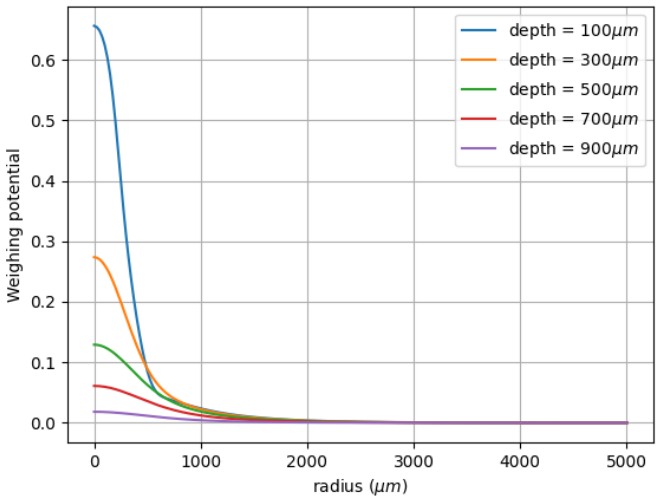


(c) Self biased surface potential

Figure 3.27: Radial electric field along drift channel

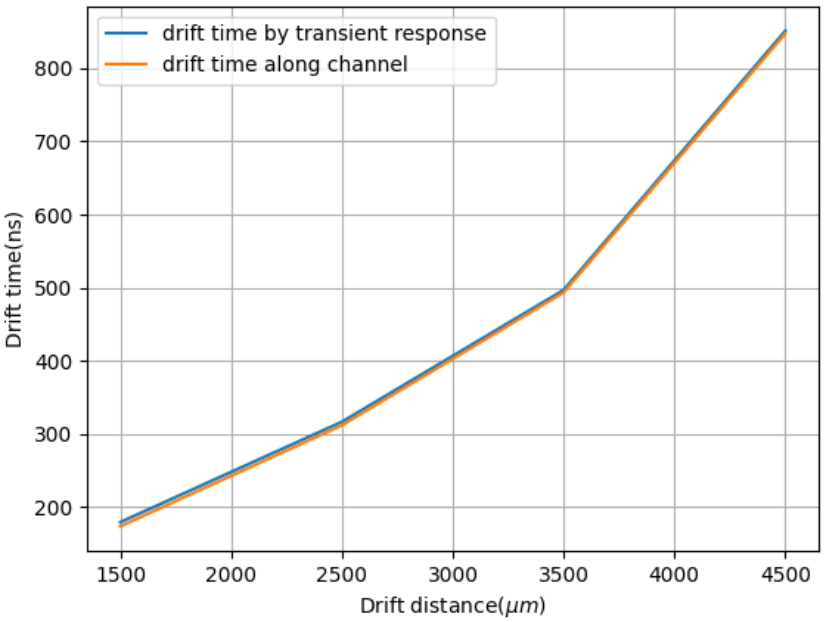


(a) Anode weighing potential contours

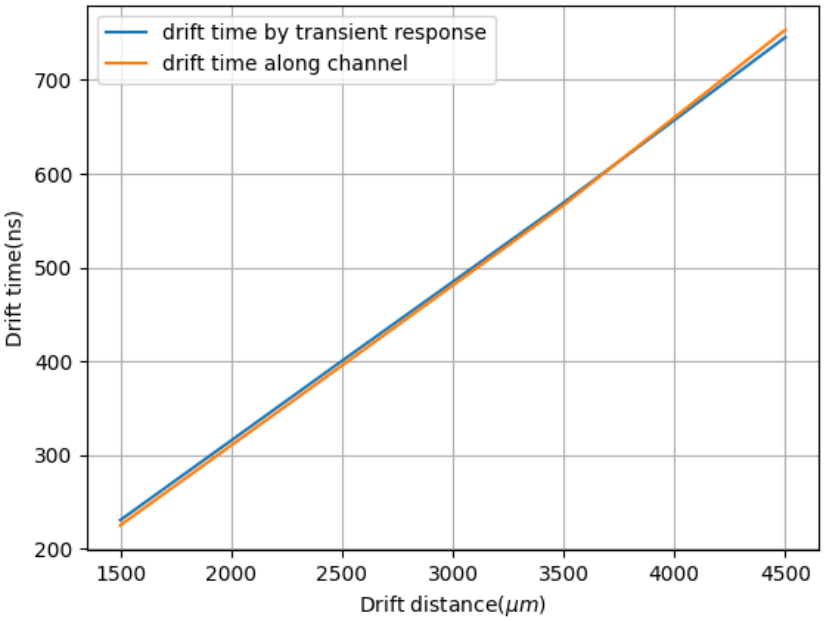


(b) Anode weighing potential at different depths in the detector

Figure 3.28: Anode Weighing Potential in the SDD

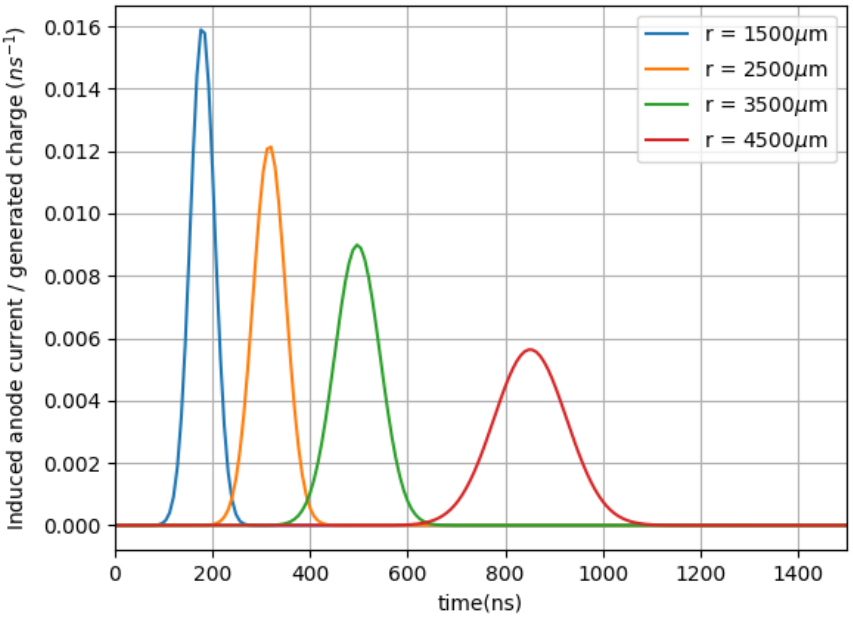


(a) Linear Potential

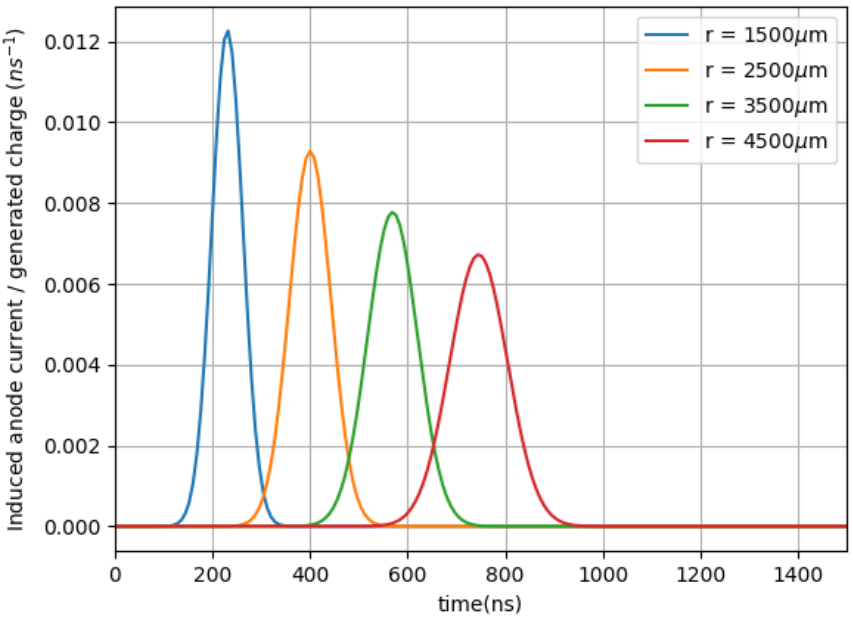


(b) Curved Potential

Figure 3.29: Drift time vs drift distance



(a) Linear Potential



(b) Curved Potential

Figure 3.30: Induced anode current per unit generated charge by triangular pulse of width 0.1 ns for different drift distance

Chapter 4

Summary and Future Work

In this thesis, a large area cylindrical silicon drift detector is designed considering various biasing schemes and geometric structure parameters to achieve minimal capacitance and minimal drift time for carriers.

4.1 Summary

- For a given SDD area, variation of capacitance with anode radius can be expressed by an effective area. Effective area and anode area are found to be related by a factor $(k_1 \frac{d}{r} + k_2)$.
- Punch through breakdown is the limiting criterion for bias voltages on SDD. Proper biasing needs to be done to use complete range of bias allowed without causing punch through between top and bottom p+.
- Concept of drift channel is introduced to estimate drift time and mean drift field. Drift channel is an electric field line with high electron density along it. As electric field lines start from n+ anode along the channel and diverge toward the electrodes, radial drift along the drift channel is a good criterion to evaluate SDD. Radial drift field can be used as an optimality criterion for a certain bias.
- Optimal surface potential derived produces uniform field and constant surface electric field produces decreasing radial field moving outwards. It is shown that self-biased and straight line surface potential are on two different sides of the optimum surface potential.
- Using weighing potential and field described by Schokley-Ramo theorem, induced current on anode is mainly due to electrons.
- Drift time found by transient response is close to the drift time defined along the drift channel demonstrating the usefulness of drift channel.
- Uniform radial drift field produced by optimum potential leads to drift time-distance linearity which is good for position sensing.

4.2 Future Work

- To fully take advantage of low capacitance of SDD, SDD with an integrated JFET should be designed.
- A cylindrical SDD should be fabricated to confirm the results mentioned.

Appendix A

Euler-Lagrange equation solution to find optimum surface potential

Under our assumptions (drift field being radial and radial field variation negligible) , $L(\phi, \phi')$ is given by

$$L(\phi, \phi') = \frac{1}{\phi' \left(1 - \frac{\phi}{2V_{dep}}\right)}$$

as discussed in **??**.
Euler-Lagrange equation is given by

$$\frac{\partial L}{\partial \phi_n} = \frac{d}{dr}\frac{\partial L}{\partial \phi'_n}$$

Defining normalised (dimensionless) $\phi_n = \frac{\phi}{2V_{dep}}$,

$$\phi'_n = \frac{d\phi_n}{dr} = \frac{\phi'}{2V_{dep}} \; ; \; L(\phi_n, \phi'_n) = \frac{1}{2V_{dep}\ \phi'_n(1-\phi_n)}$$

$$\implies \frac{\partial L}{\partial \phi'_n} = \frac{1}{(\phi'_n)^2(\phi_n - 1)} \; ; \; \frac{\partial L}{\partial \phi_n} = \frac{1}{\phi'_n(\phi_n - 1)^2}$$

$$\frac{\partial L}{\partial \phi} = 2V_{dep}\frac{\partial L}{\partial \phi_n} \qquad ; \qquad \frac{\partial L}{\partial \phi'} = 2V_{dep}\frac{\partial L}{\partial \phi'_n}$$

Hence, Euler-Lagrange equation can be written as

$$\frac{\partial L}{\partial \phi_n} = \frac{d}{dr}\frac{\partial L}{\partial \phi'_n}$$

$$\frac{d}{dr}\frac{\partial L}{\partial \phi'_n} = -\frac{(\phi'_n)^2 + 2\phi''_n(\phi_n - 1)}{(\phi'_n)^3(\phi_n - 1)^2}$$

$$\implies \frac{1}{\phi_n'(\phi_n-1)^2} = -\frac{(\phi_n')^2 + 2\phi_n''(\phi_n-1)}{(\phi_n')^3(\phi_n-1)^2}$$

$$\implies (\phi_n')^2 + \phi_n''(\phi_n-1) = 0$$

Defining $\phi_t = 1 - \phi_n$,

$$\begin{aligned} \phi_t' = -\phi_n' \ ; \ \phi_t'' = -\phi_n'' \\ \implies (\phi_t')^2 + \phi_t''\phi_t = 0 \\ \implies \phi_t' \frac{d\phi_t}{dr} + \frac{d\phi_t'}{dr}\phi_t = 0 \\ \implies \frac{d}{dr}(\phi_t'\phi_t) = 0 \end{aligned}$$

Integrating with respect to r, we get

$$\phi_t\phi_t' = A$$

for integration constant A

$$\implies \phi_t \frac{d\phi_t}{dr} = A$$

Integrating again with respect to r, we get

$$\begin{aligned} \int \phi_t \ d(\phi_t) = \int A \ dr \\ \implies \frac{\phi_t^2}{2} = Ar + B \end{aligned}$$

for integration constant B

$$\implies \phi_t = \sqrt{\alpha r + \beta}$$

for some constants α and β

$$\begin{aligned} \implies \phi_n = 1 - \phi_t = 1 - \sqrt{\alpha r + \beta} \\ \implies \phi = 2V_{dep}\phi_n = 2V_{dep}(1 - \sqrt{\alpha r + \beta}) \end{aligned}$$

Setting $\phi(0) = 0$, we get $\beta = 1$.

$$\implies \phi = 2V_{dep}(1 - \sqrt{\alpha r + 1})$$

Setting $\phi(R) = 2V_{dep}$, we get $\alpha = \frac{-1}{R}$.

$$\implies \phi = 2V_{dep}\left(1 - \sqrt{1 - \frac{r}{R}}\right)$$

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