Silicon Drift Detectors

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Outline

Absorption efficiency (η)

- X-rays absorbed in Si generates e-h pairs
- Fraction of photons absorbed depend on α

$$\eta = (1 - e^{-\alpha x})$$

- Wafer with thickness 1 mm suitable for energy upto 20 keV

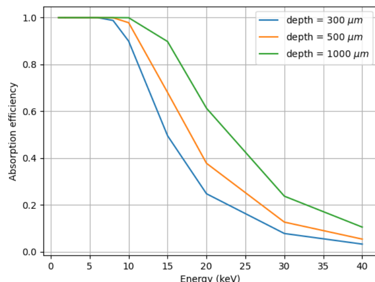
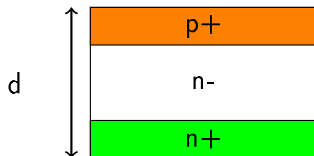


Figure 1: Absorption efficiency increasing with wafer thickness

PIN diode



- High reverse bias applied to p+ to fully deplete it and generate electric field

$$V_{depletion} = q\frac{N_D d^2}{2\epsilon_{Si}}$$

- Top and bottom are highly doped to form good ohmic contact
- High doping also ensures low diffusion current
- Top p+ and n+ implantation depth are kept small to keep dead volume low

Need for SDD

- At full depletion, capacitance saturates to a minimum value and is given

$$C = \frac{A\epsilon_{Si}}{W_{detector}}$$

- C is proportional to the area which becomes very high for large area detectors.For $A = 50mm^2$ and $d = 1mm$, C $\approx$ 50 pF
- Not suitable for low noise detection

Working of SDD

- n+ contact can be made small and placed on top
- Remaining space on top can be covered by p+ to deplete the bulk

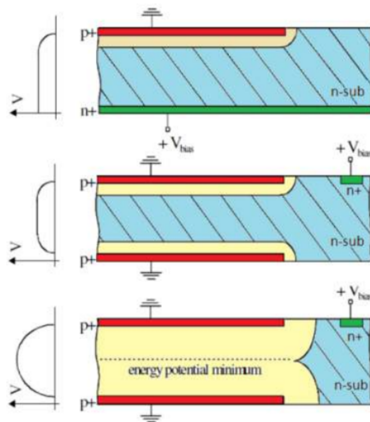


Figure 2: Structure demonstrating sideward depletion.?

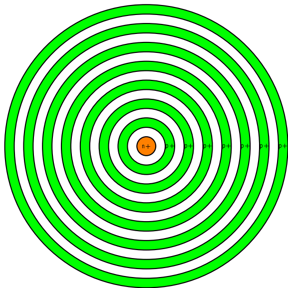


Figure 3: Top view of cylindrical SDD

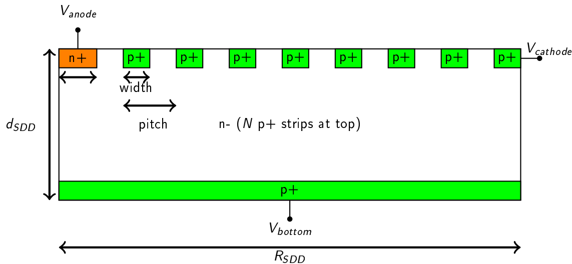


Figure 4: Radial cross-section of cylindrical SDD

Potential gutter

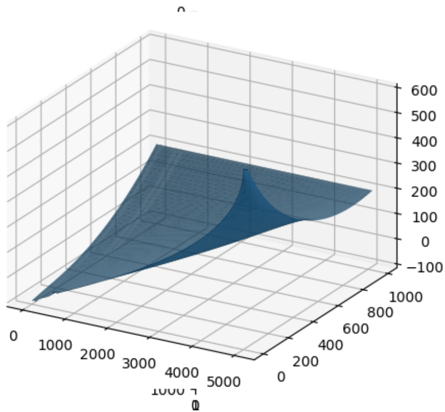


Figure 5: Electron (Negative) Potential in SDD

Goals

For high SNR, C and leakage current should be low.

- C $<$ 100 fF
- Leakage current below 100 nA at room temperature
- Low drift time (High radial field)
- Device area $= 0.8\ cm^2$ ($R = 5mm$, $d = 1mm$)

Key Design elements

- **Anode width**: Decides the anode capacitance
- **Biasing Range**: Range of allowed bias to maximise field
- **Surface potential**: Ensure uniform radial drift field

Anode capacitance

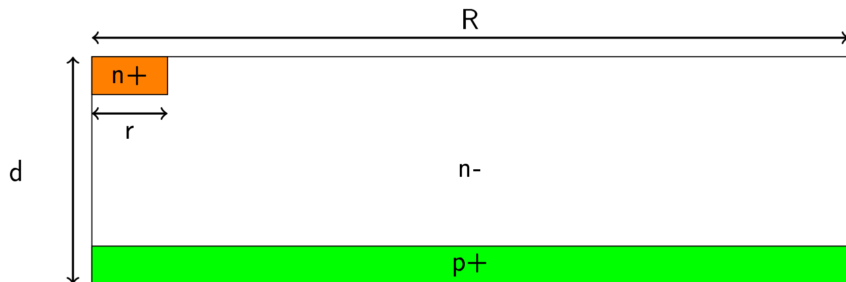
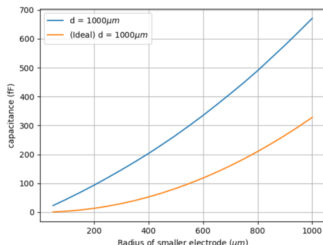


Figure 6: Structure considered for capacitance simulation

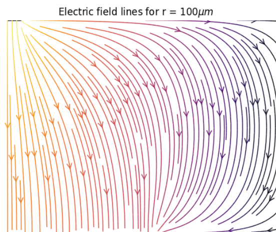
Parallel plate capacitor

$$C = \epsilon \frac{A}{d} = \epsilon \frac{\pi r^2}{d}$$

- True for $r >> d$
- For small r/d, fringing effects become dominant



(a) Real capacitance

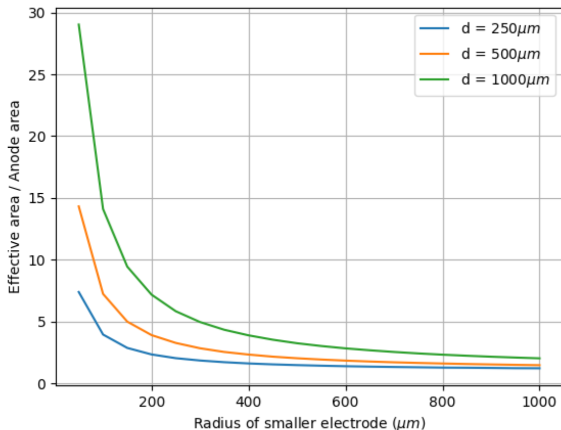


(b) fringe

Parallel plate capacitor

- Capacitance increase due to fringing is expressed by $A_{effective}$

$$C_{real} = \epsilon \frac{A_{effective}}{d}$$



Parallel plate capacitor

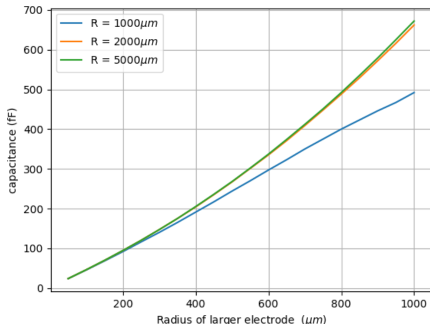


Figure 9: Capacitance is relatively independent of R while d is much smaller than R

- For large R/d, fringe field don't cross boundary of larger plate
- Geometric similarity means $\frac{A_{effective}}{A_{anode}} = f\left(\frac{r}{d}\right)$

Anode capacitance

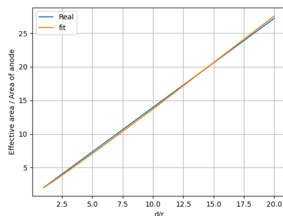


Figure 10: $\frac{A_{effective}}{A_{anode}}$ varies linearly with d/r

$$A_{eff} = A_{anode}(k_1 \frac{d}{r} + k_2)$$

where $k_1 = 1.32$ and $k_2 = 0.73$

- Anode capacitance about 45 fF for $r = 100\mu m, d = 1mm, R = 5mm$
- $r = 100\mu m$ is chosen as anode radius

Material Parameters

- **Substrate**: n-Silicon $\rho = 10k\Omega - cm$ ($N_D = 5 \times 10^{11}/cm^3$). $V_{dep} \approx 380V$
- **Doping**: Magnitude of doping of $n+$ and $p+$ regions is $10^{18}/cm^3$.
- **Carrier lifetime**: High-lifetime(>1 ms) Si wafer for low generation current.$\tau_n = \tau_p = 1ms$
- **Carrier mobility**: $\mu_n = 1000V - cm^2/s$, $\mu_p = 500V - cm^2/s$

Biasing schemes

- Two possible schemes
- Voltage divider made by poly-Si resistors on top
- Intermediate strips left unbiased

Structure with poly-silicon on top

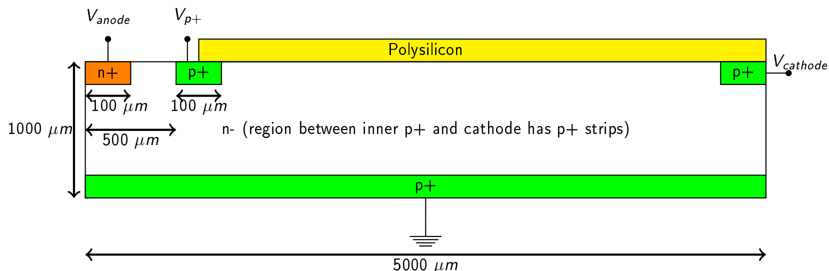


Figure 11: SDD structure considered for simulation (Left edge represent axis of cylindrical structure (r=0))[Poly Resistance = 20 ohm/um]]

Self biased structure

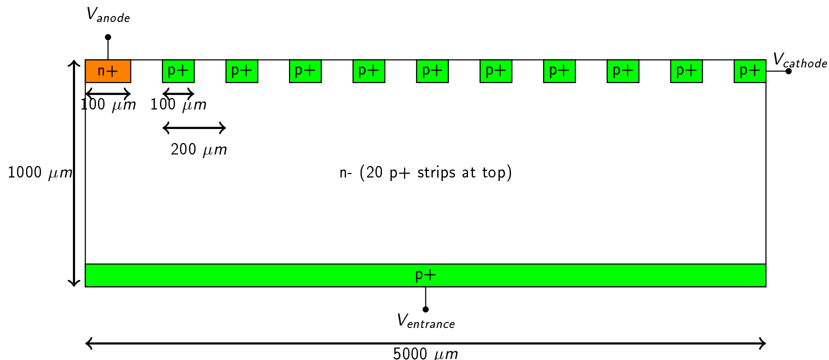


Figure 12: Self-biased SDD structure considered for simulation (there are 25 p+ strips at top and shallow p+ layer at the entrance)

Depletion

- High +ve bias to anode, all other electrodes grounded
- At full depletion,leakage current saturates to 94 nA

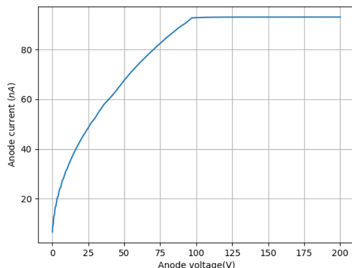


Figure 13: Anode leakage current

- Leakage current is due to thermal generation (seen by $\sqrt{V}$ relation)

Generating drift field

- Generate highest drift possible
- Maintain depletion from breaking
- Punch through breakdown is the limiting factor

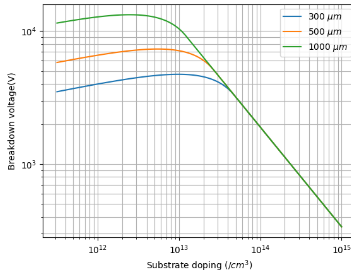


Figure 14: Avalanche breakdown voltage (PIN diode)

Punch through breakdown

- Consider a vertical section in SDD crossing p+ strip at top and p+ layer at bottom
- Since whole n- is depleted, both p+-n junctions are reverse biased
- This is different from punch-through in p-n-p BJTs where one p-n junction is forward biased

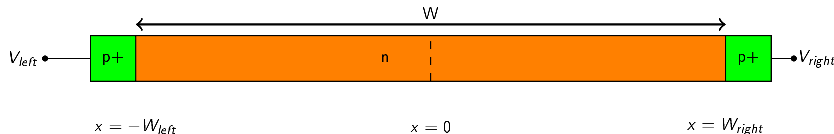


Figure 15: One dimensional section of a p+-n-p structure

Potential profile for p+n-p structure

$$\nabla . \vec{E} = -\frac{d^2 V}{dx^2} = \frac{qN_D}{\epsilon}$$
$$V_{left} \geq V_{right}$$

- $\frac{qN_D}{\epsilon}$ is the curvature of potential

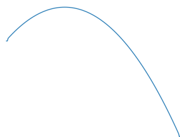


Figure 16: Potential profile of p+-n-p structure showing potential barrier for holes (Left end is $x = -W_{left}$ and right end is $x = W_{right}$)

Punch through breakdown

$$\Delta V = V_{left} - V_{right} \tag{1}$$

$$W_{left} = \frac{W}{2} - \frac{\epsilon \Delta V}{q N_D W}; W_{right} = \frac{W}{2} + \frac{\epsilon \Delta V}{q N_D W} \tag{2}$$

- As +ve bias on left end is increased, the barrier moves towards left and starts decreasing in height
- Punch-through breakdown occurs when barrier reaches other as barrier becomes small enough

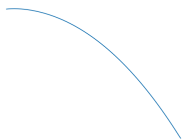


Figure 17: Potential profile of p+-n-p structure showing potential barrier for holes (Left end is $x = -W_{left}$ and right end is $x = W_{right}$)

Punch-through breakdown

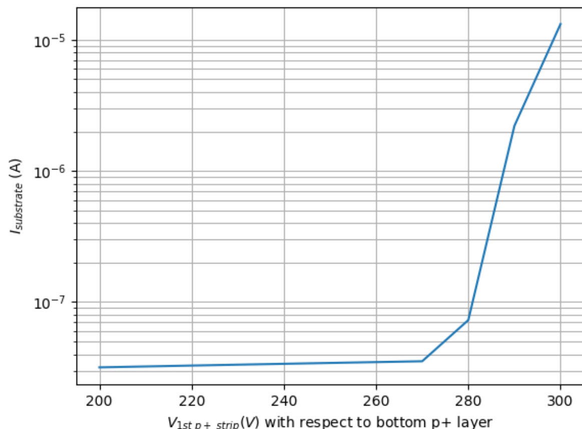


Figure 18: Punch through breakdown occuring at about 270 V difference between inner p+ strip and bottom p+ ($V_{dep} \approx 380V$)
[$V_{n+} = 300V$, $V_{righttopp+strip} = -350V$, $V_{bottomp+} = 0V$

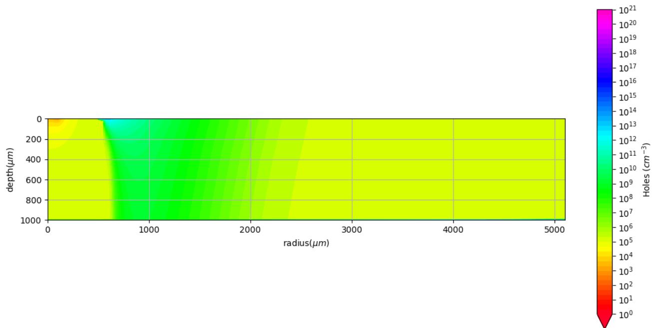


Figure 19: Holes being injected from inner p+ strip breaking down depletion (Voltage difference between top and bottom p+ is 300 V)

Revisiting punch-through breakdown analysis

- Radial field variation can't be neglected
- In one-dimensional analysis, all donor dipoles align vertically
- But, all donor dipoles cannot be completely vertical in presence of radial field

Revisiting punch-through breakdown analysis

$$\nabla.\vec{E} = \frac{1}{r}\frac{\partial(rE_r)}{\partial r} + \frac{\partial E_z}{\partial z} = \frac{E_r}{r} + \frac{\partial E_r}{\partial r} + \frac{\partial E_z}{\partial z} \tag{3}$$

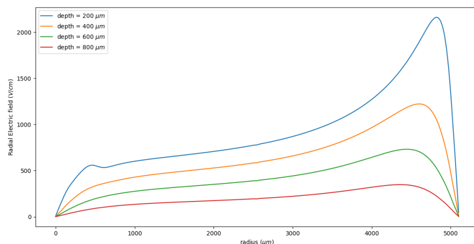


Figure 20: Radial field variation

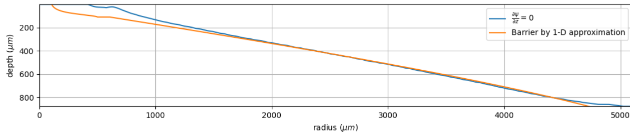


Figure 21: Potential barrier position is more closer to the inner p+ than barrier position given by (**??**).Potential barrier position is farther from bottom p+ layer than barrier position given by (**??**).[Barrier position is plotted for structure when breakdown occurs at inner p+.]

Breakdown voltage decreases for inner p+ strip and increase for outer p+ strip

Final bias voltage

- Voltage divider on top

$$
\begin{aligned}
V_{anode} &= 300V \\
V_{cathode} &= -400V \\
V_{p+} &= 250V \\
V_{bottom} &= 0V
\end{aligned}
$$

- Self biased

$$
\begin{aligned}
V_{anode} &= 350V \\
V_{cathode} &= -400V \\
V_{bottom} &= 0V
\end{aligned}
$$

Surface potential

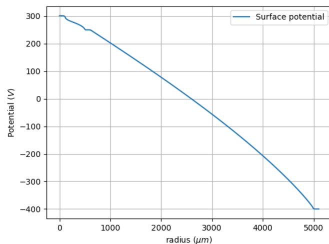
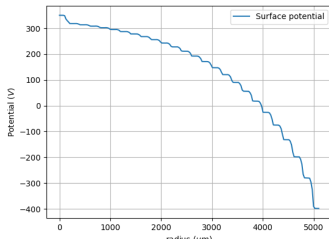


Figure 22: Linear surface potential



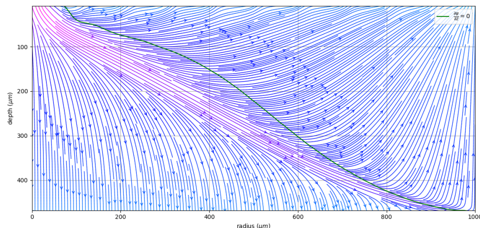
Design Evaluation

- Radial drift field along
- Collection efficiency
- Transient behaviour

Drift channel

- **Channel** : A pathway for electrons
- In semiconductors, $\vec{v} || \vec{E}$
- Center of charge cloud moves along an electric field line
- Drift channel should be an electric field line
- Drift path defined by P. Rehak. et. el(1989):

$$\left(\frac{\partial V}{\partial z}\right)_{z=z(r)} = 0$$



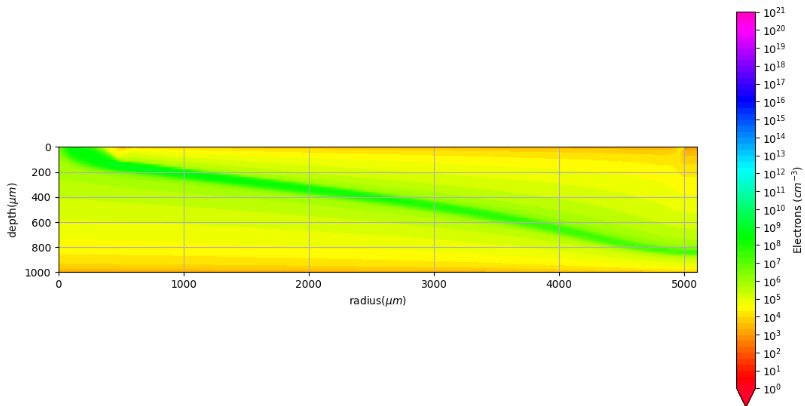
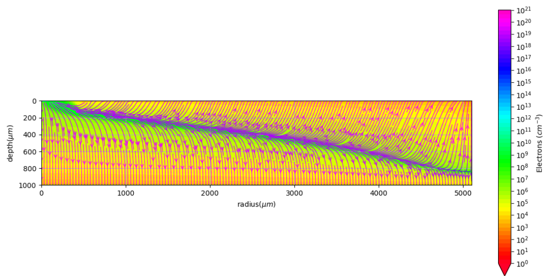
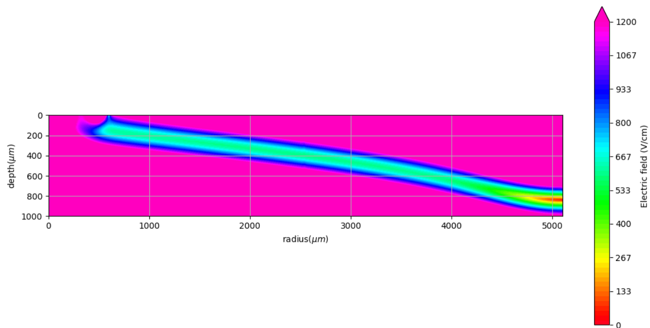
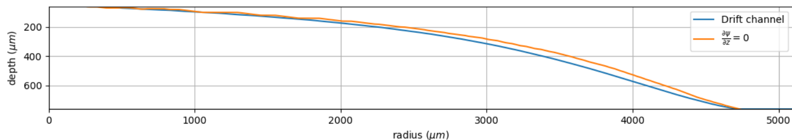


Figure 24: High electron density channel

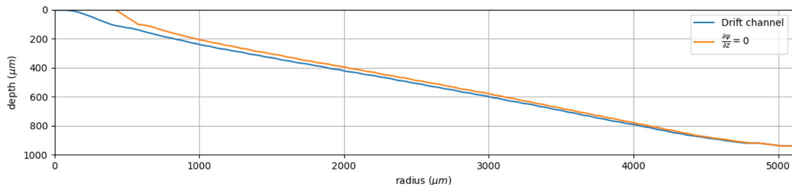

depth(μm)
radius(μm)
Electrons (cm^{-3})


depth(μm)
radius(μm)
Electric field (V/cm)

Drift channel shape



(a) Self-biased surface potential leading to curviest drift channel



(b) Linear surface potential leading to straight drift channel

Figure 25: Drift channel for different surface potentials

Drift time

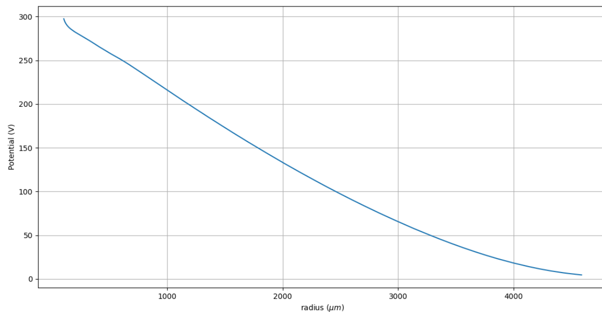
$$t = \int_{r_0}^{r} \frac{dr}{v_{drift,r}} = \int_{r_0}^{r} \frac{dr}{\mu_n \; E_{drift,r}} = \frac{r - r_0}{\mu_n \; E_{drift,mean}}$$

$$E_{drift,mean} = \frac{r - r_0}{\int_{r_0}^{r} \frac{dr}{E_{drift,r}}}$$

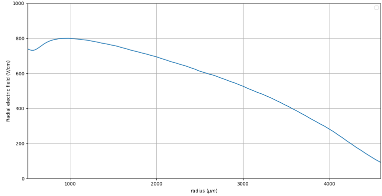
- Lower electric field regions slow down the carriers and take much of the carrier's drift time
- Mean drift field closer to minimum electric field than maximum.
- $\implies$ For a given potential difference, optimum drift field should be uniform

Maximum drift field

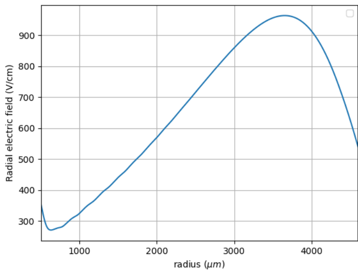
$$\left(E_{drift,mean}\right)_{max} = \frac{V_{anode} - V_{bottom}}{R}$$



Drift field



(a) Linear surface potential



(b) Self biased surface potential

- **Straight line potential**: Decreasing field (Low resistance poly)
- **Self biased potential**: Increasing field (No poly -> Infinite resistance)
- Optimum in between
- As channel moves away from n-side (top), effect of surface field diminishes.
- To counter it, increasing surface field is required.

Surface potential

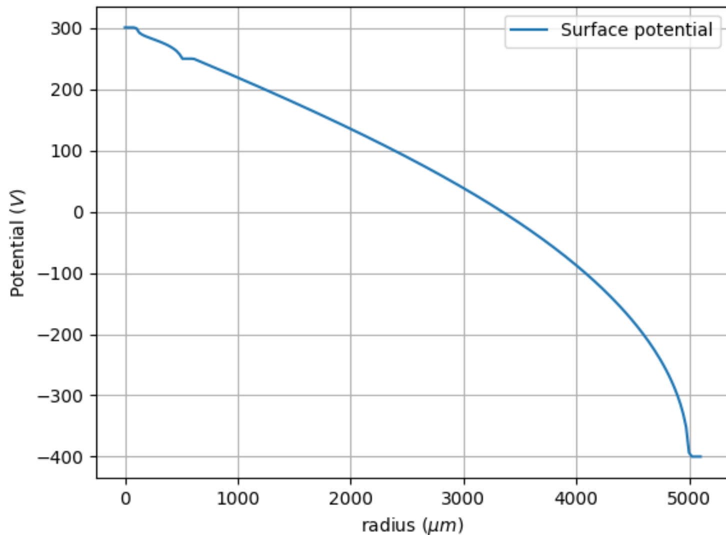


Figure 27: Optimum surface potential

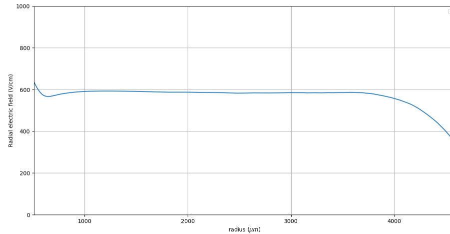


Figure 28: Radial drift field along the channel for curved surface potential

Optimum drift field

$$\phi(r) \propto \left(\sqrt{1-\frac{r}{R}}-1\right)$$

$$z_{dr}(r) = d\left(1-\sqrt{1-\frac{r}{R}}\right)$$

$$E_{surface,r} = -\frac{d}{dr}\phi(r) \propto \frac{1}{\sqrt{1-\frac{r}{R}}}$$

- Results in uniform radial drift field
- Diverging electric field at surface

Optimum surface field

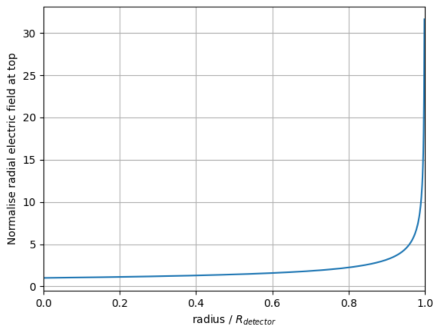
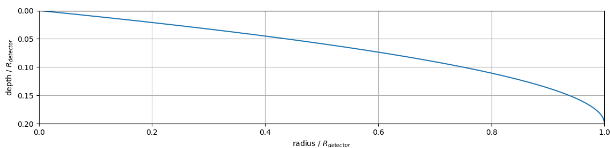


Figure 29: Surface electric field leading to curved optimum drift channel



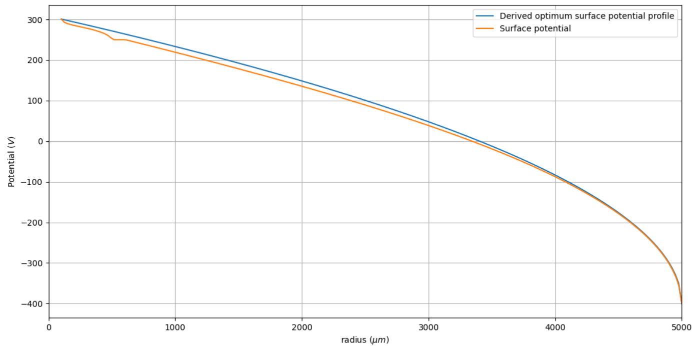
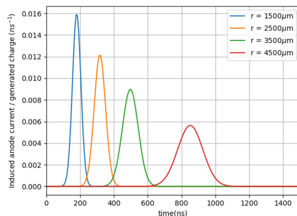


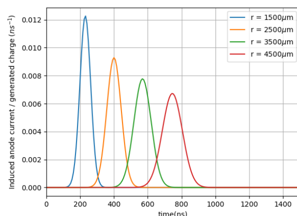
Figure 31: Comparison

Transient pulse

- Triangular pulse of width $0.1ns$ incident at different radial distance



(a) Linear Potential



Interpretation using Shockley-Ramo Theorem

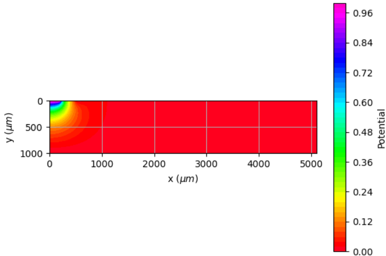
$$Q = -q\ \phi_0(\mathbf{x})$$
$$i = -q\ \vec{v}.\vec{E_0}(\mathbf{x})$$

- Weighing potential is a solution of Laplace equation

$$\nabla^2\phi = 0$$
$$\phi(anode) = 1, \phi(p+\ \ strips) = \phi(bottom\ p + layer) = 0$$

- Only depends on geometry of the biased electrodes (Independent of applied bias and space charge)
- As charge moves, it gains kinetic energy by energy stored in electric field
- To restore that, power supplies push more energy which leads to induced charge

Interpretation using Shockley-Ramo Theorem



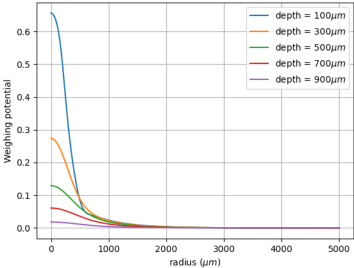
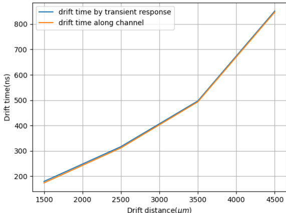
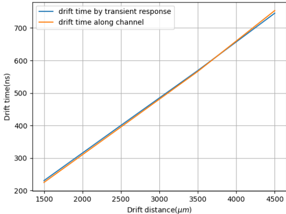


Figure 33: Anode weighing potential at different depths in the detector

Drift time-distance



(a) Linear Potential



(b) Curved Potential

Surface potential	Mean drift field [V/cm] (extracted from transient response)	Mean drift fielc (by integrat
Curved	604	598
Straight	529	531

Table 1: Mean drift field comparison

Manufacturability

- Poly-Si resistors: Resistance for optimum case $\approx$ 49 ohms/um
- For 10 μm width, $R_{sheet} \approx 490\ \Omega/square$
- With 250 nm thickness, doping $\approx 10^{19}/cm^3$

Summary

- Linear relation between $A_{effective}/A_{anode}$ and d/r to determine anode radius
- Analysis of punch through accounting radial flux
- Drift channel with appropriate definition
- Mean drift field and Drift time to evaluate device
- Optimum surface potential by optimising resistance of voltage divider
- Weighing potential given by S-R theorem to understand induced current on anode
- SDD of radius 5 mm and depth 1 mm (94 nA, c $\approx$ 48 fF and mean drift field of 598 V/cm)

Future Work

- Design for lower R/d
- Integrate JFET with SDD
- Fabricate SDD